Programming Management Unit: Open-Source Core for Secure FPGA Bitstream Configuration

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Open-Source Computer Architecture Research 2023

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Motivation

- FPGAs are essential to modern high-performance systems

Wired and wireless communications

Audio and video broadcasting

Data center

[Author's Own]

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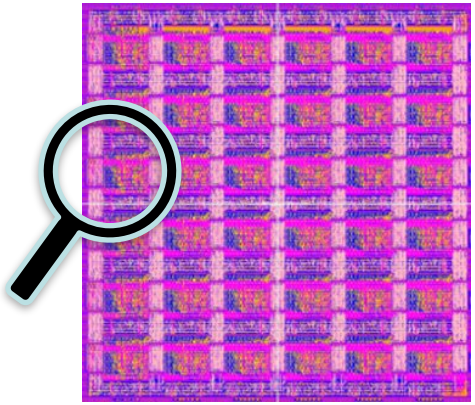
- Prime target for adversaries



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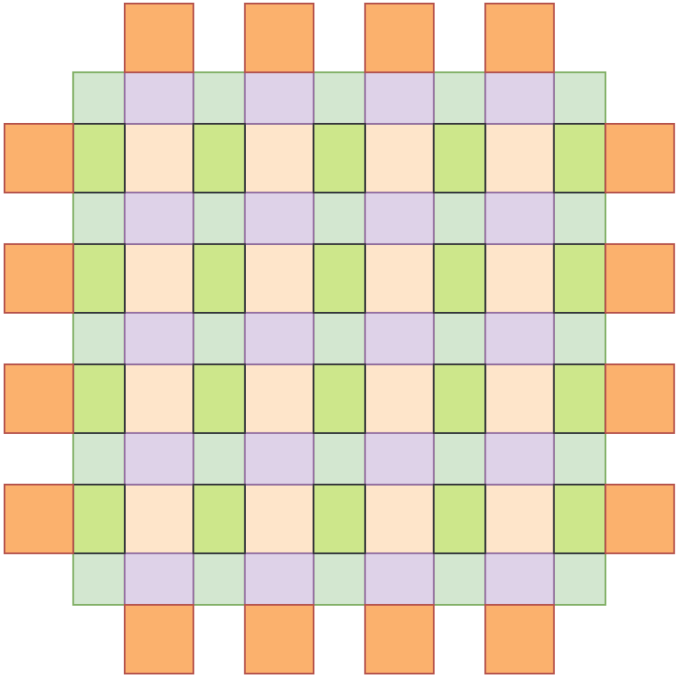
- Configurable architectures are generic in nature



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- Configurable architectures are generic in nature
- FPGAs are programmed with user IP

```
module adder_16bit(
  input [15:0] a,
  input [15:0] b,
  output [15:0] sum
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    assign sum = a + b
  endmodule
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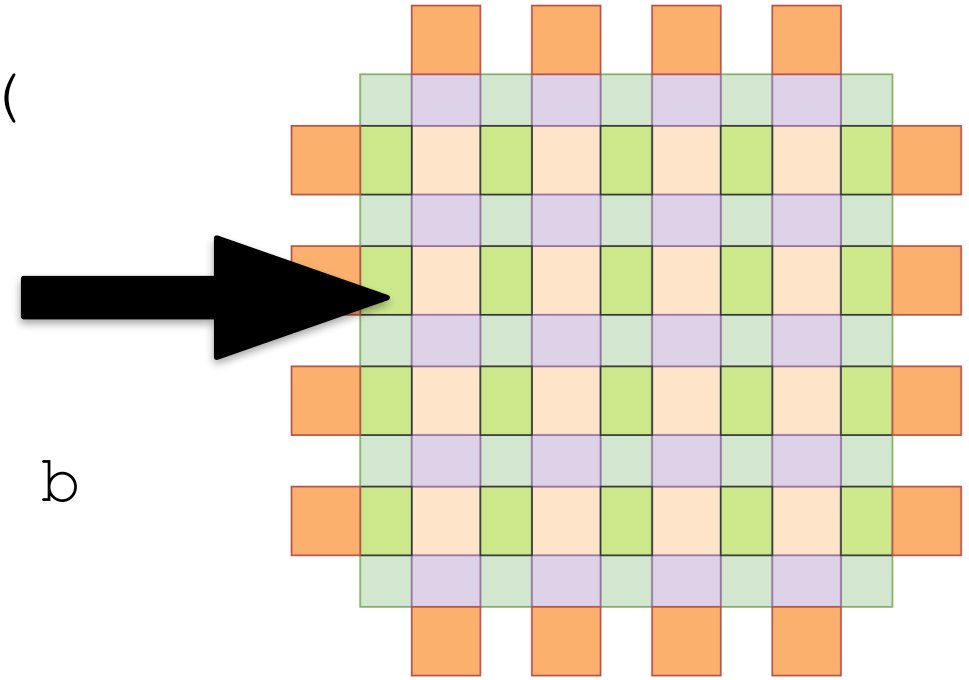

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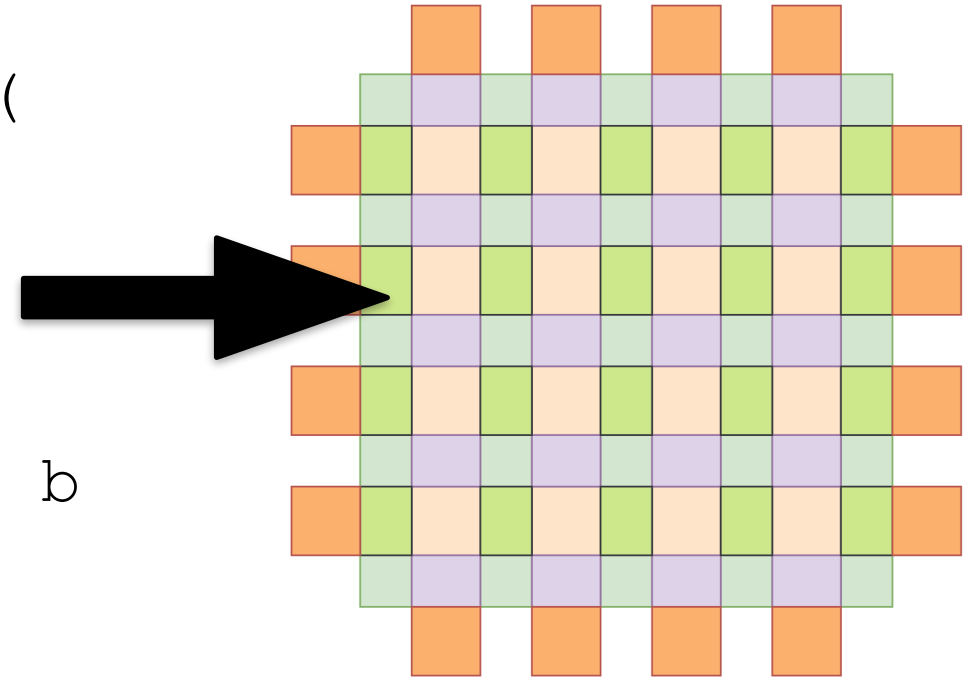
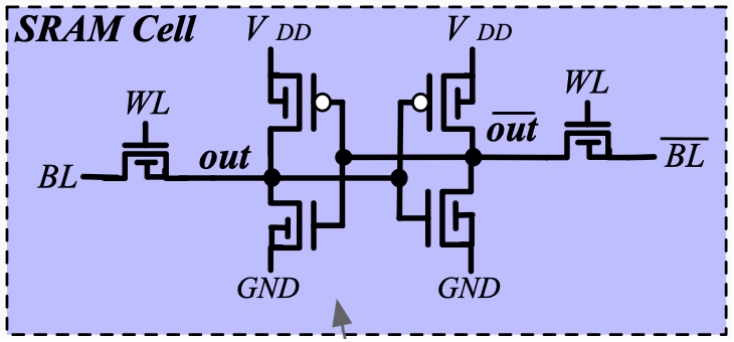


Essential to essential to safeguard the configuration data

FPGA Configuration Protocol

- State-of-the-art FPGAs leverage SRAM-based configuration
  - High speed, low power, scalable



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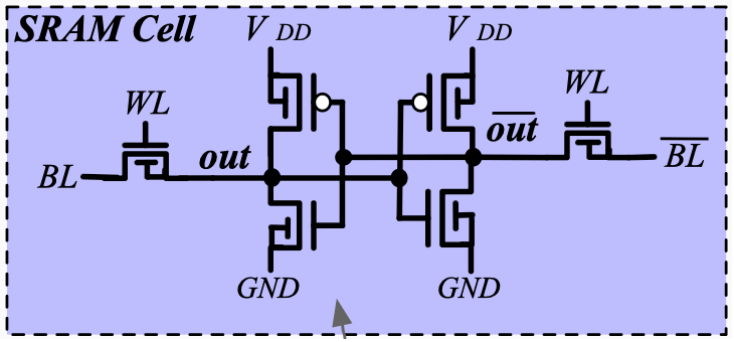

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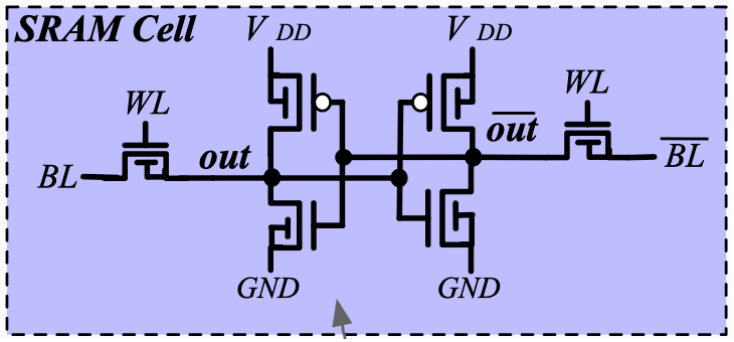

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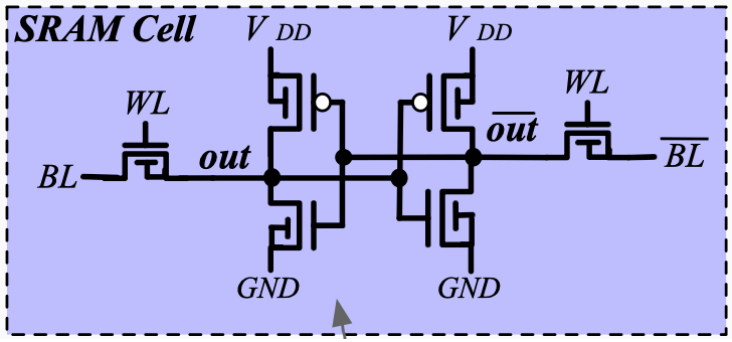
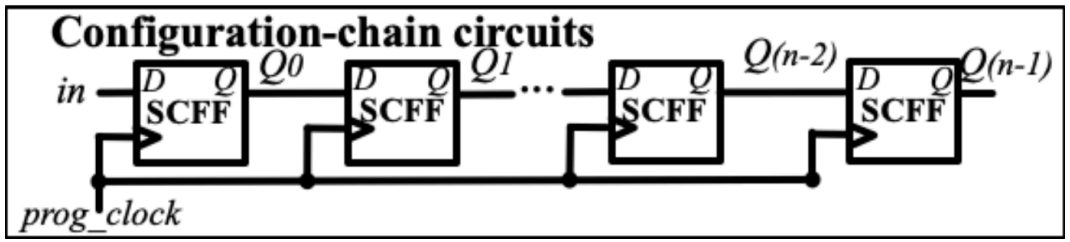
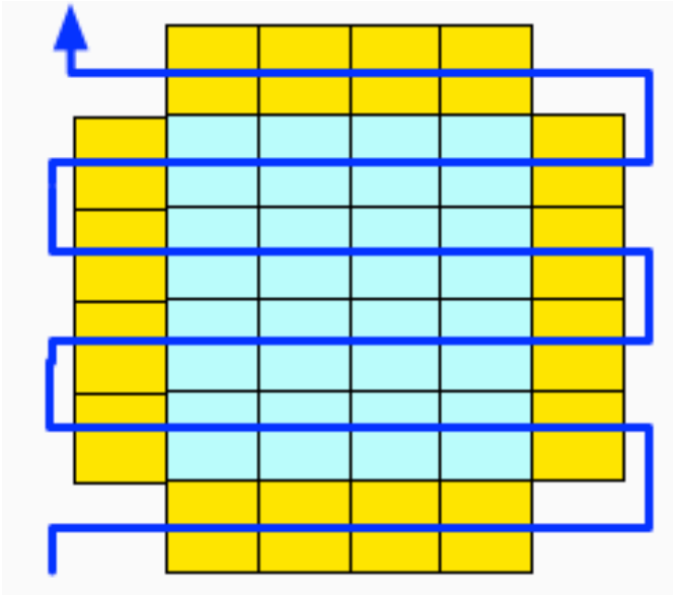
- PMU targets a OpenFPGA serial configuration-chain protocol



OPEN FPGA





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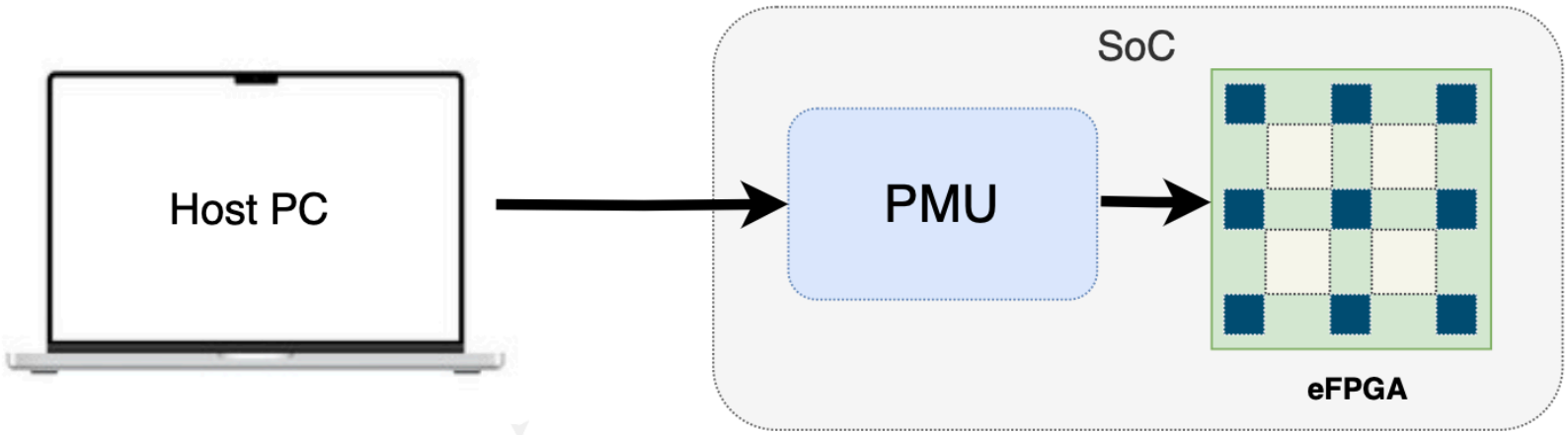
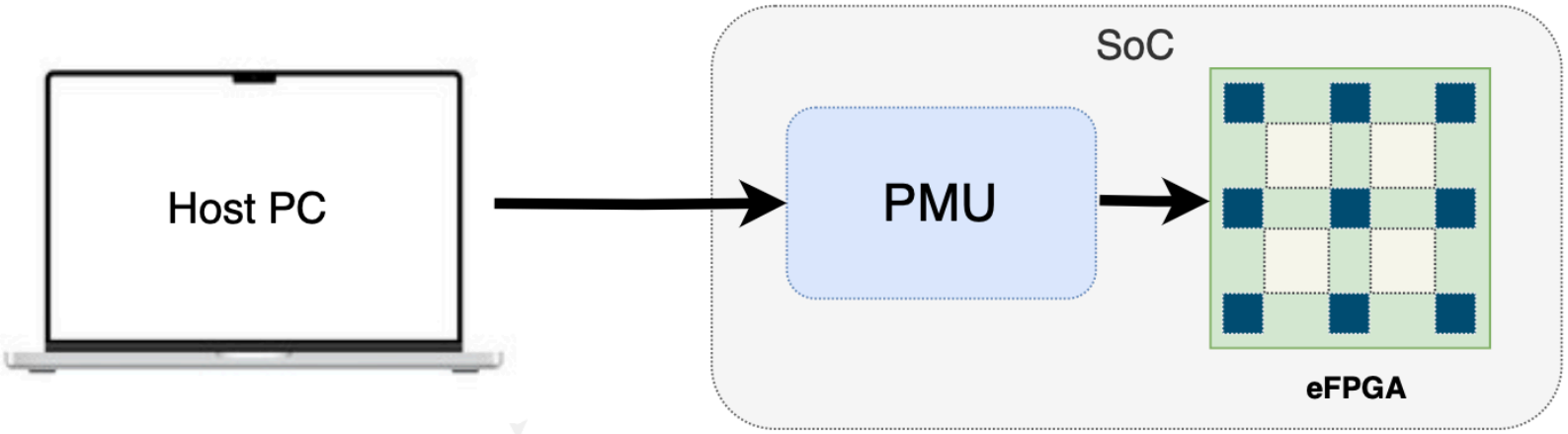
- **Proposal:**
  - First open-source IP core specifically dedicated to FPGA configuration
  - Customizable framework dedicated to secure data movement from EDA bitstream generation to FPGA core configuration circuitry.



PMU Threat Model

- PMU bitstream security measures constrained to “at-rest” and “loading” stages of configuration procedure



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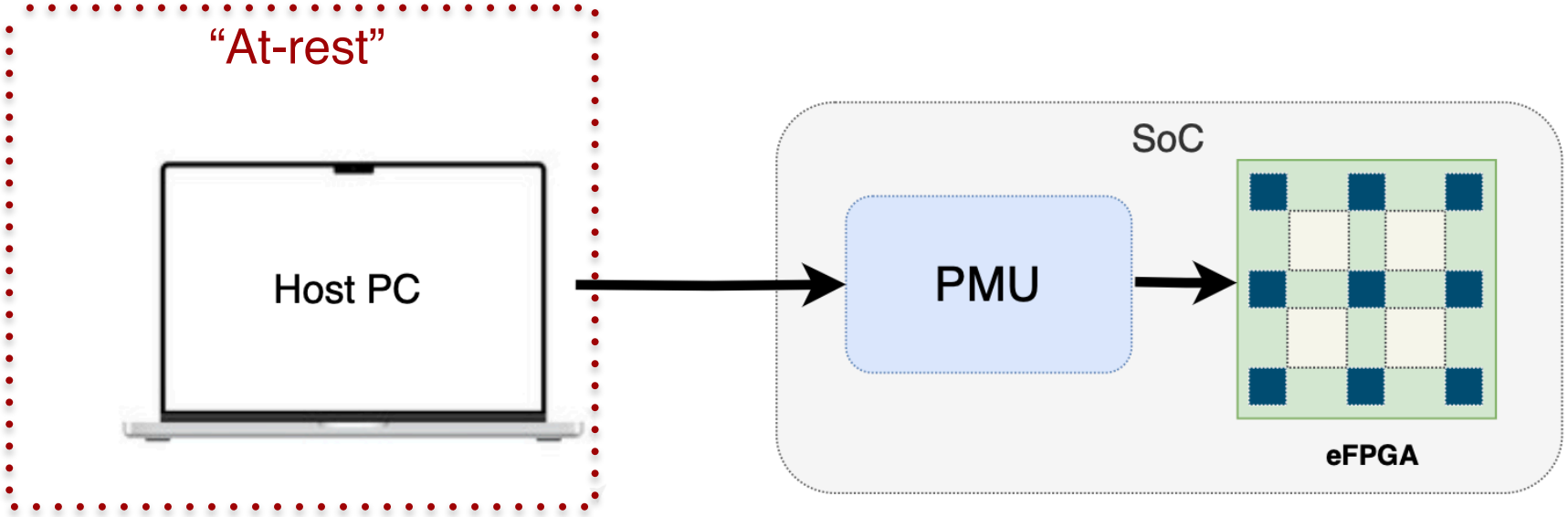

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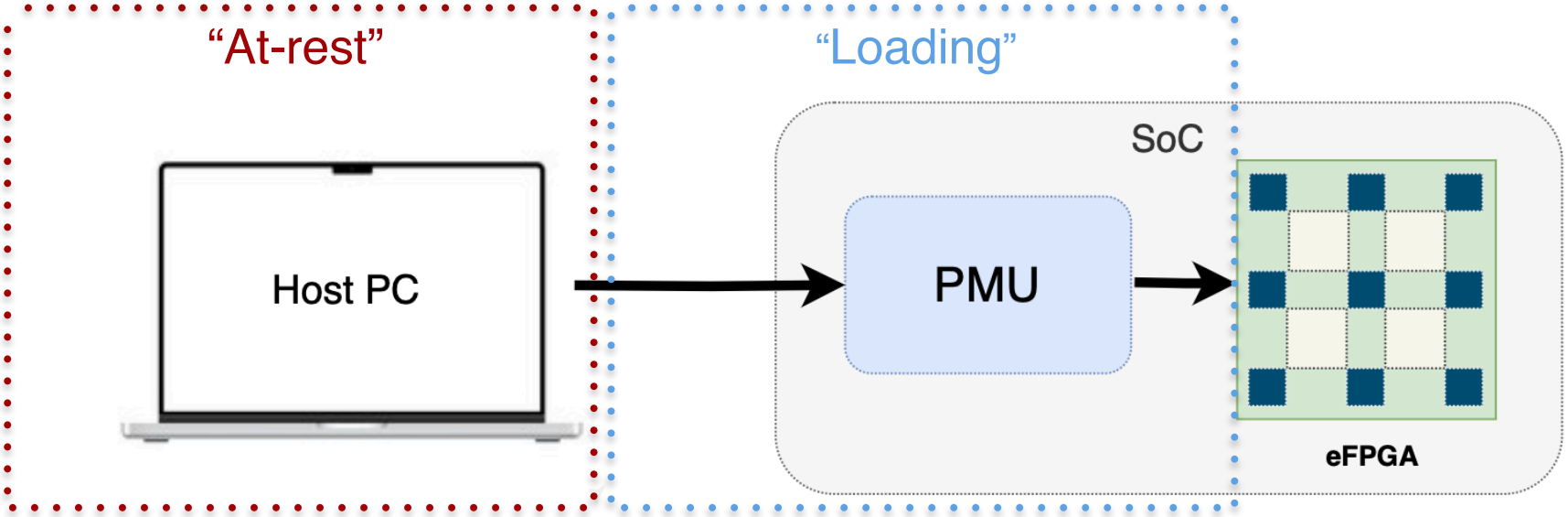

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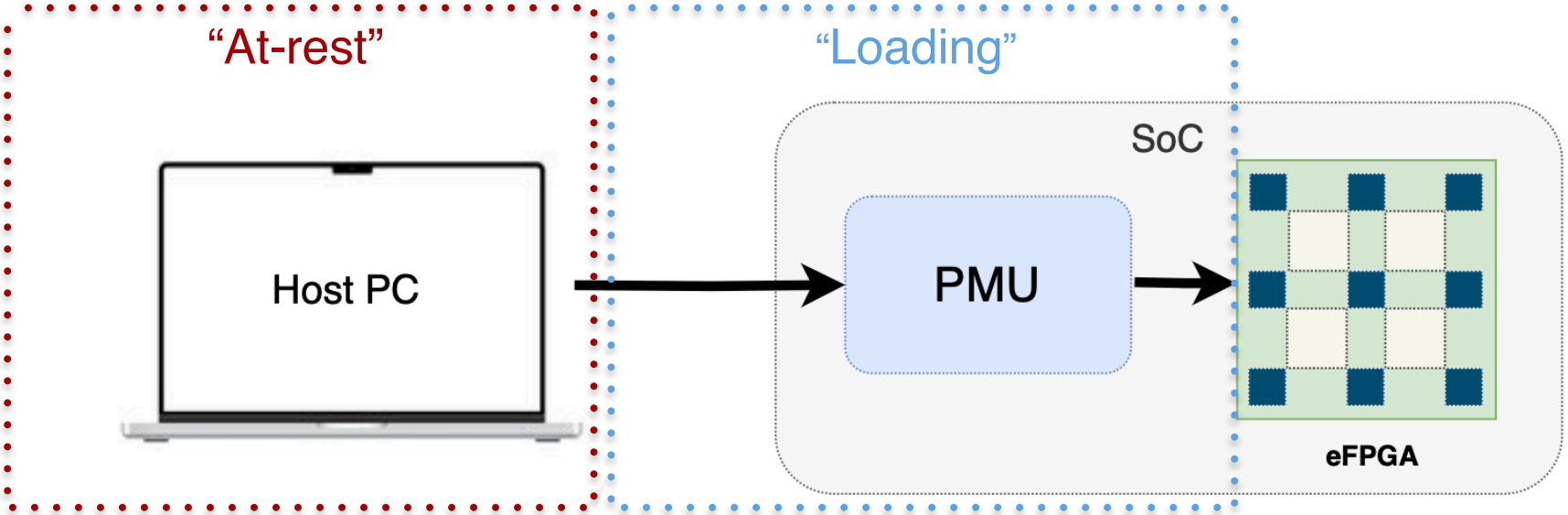
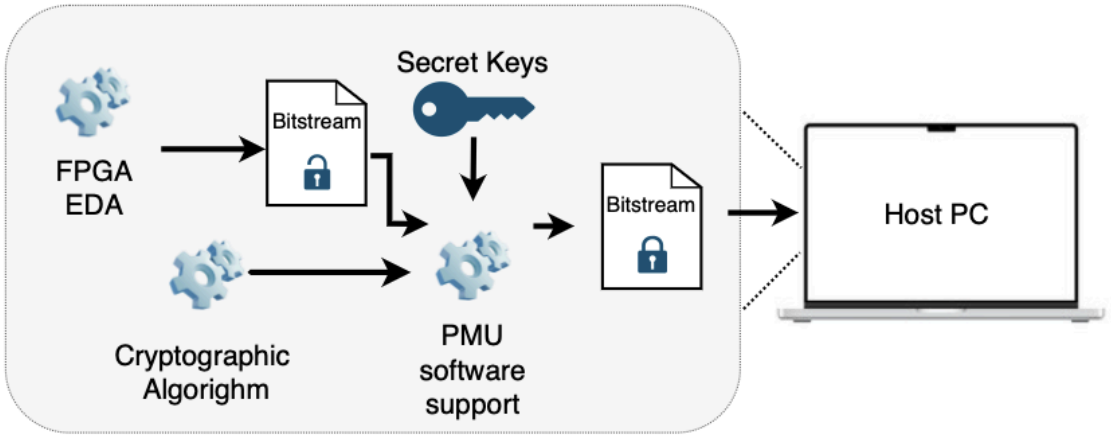


- Key storage falls outside the scope of work for this project.

Proposed System Architecture



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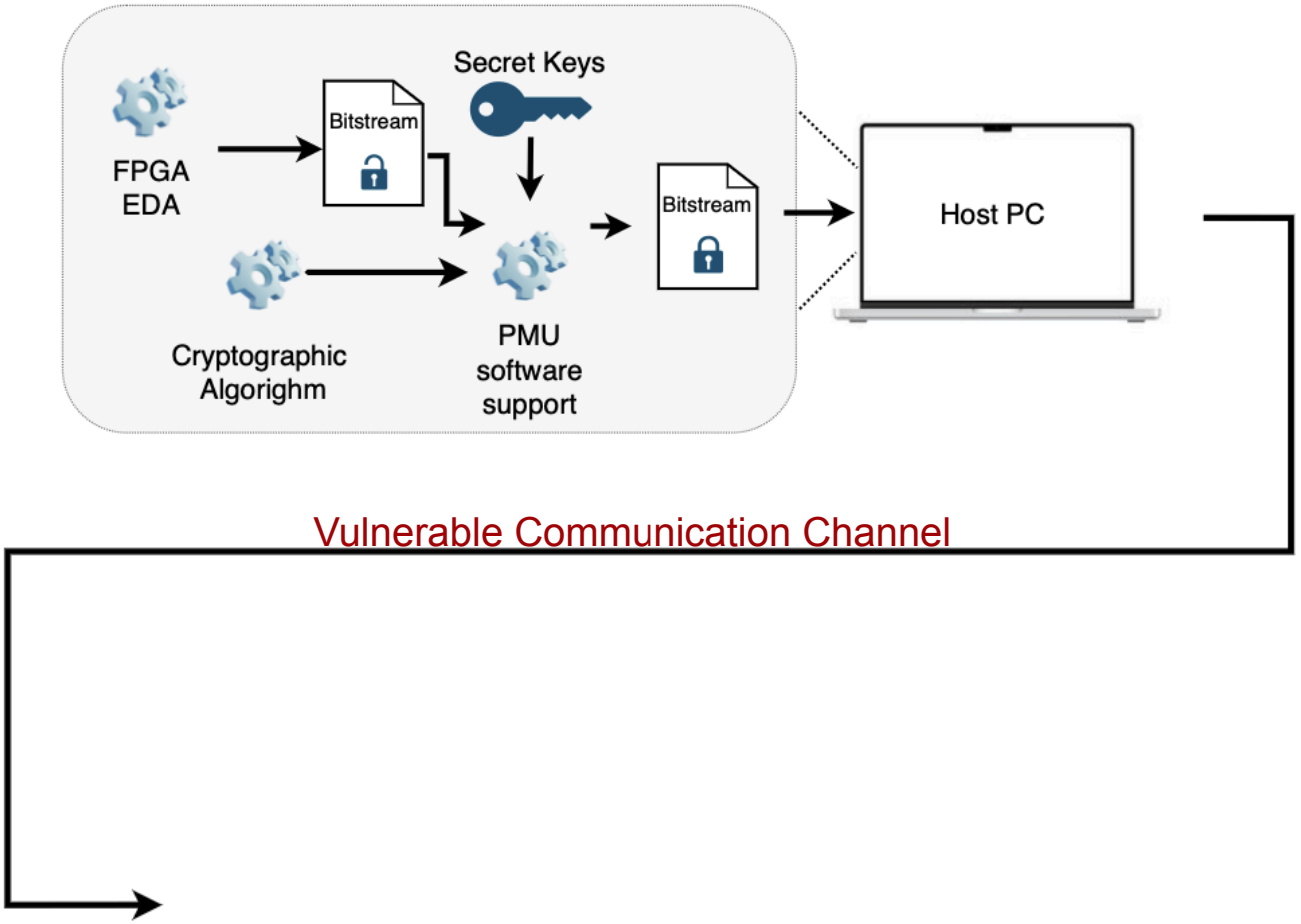

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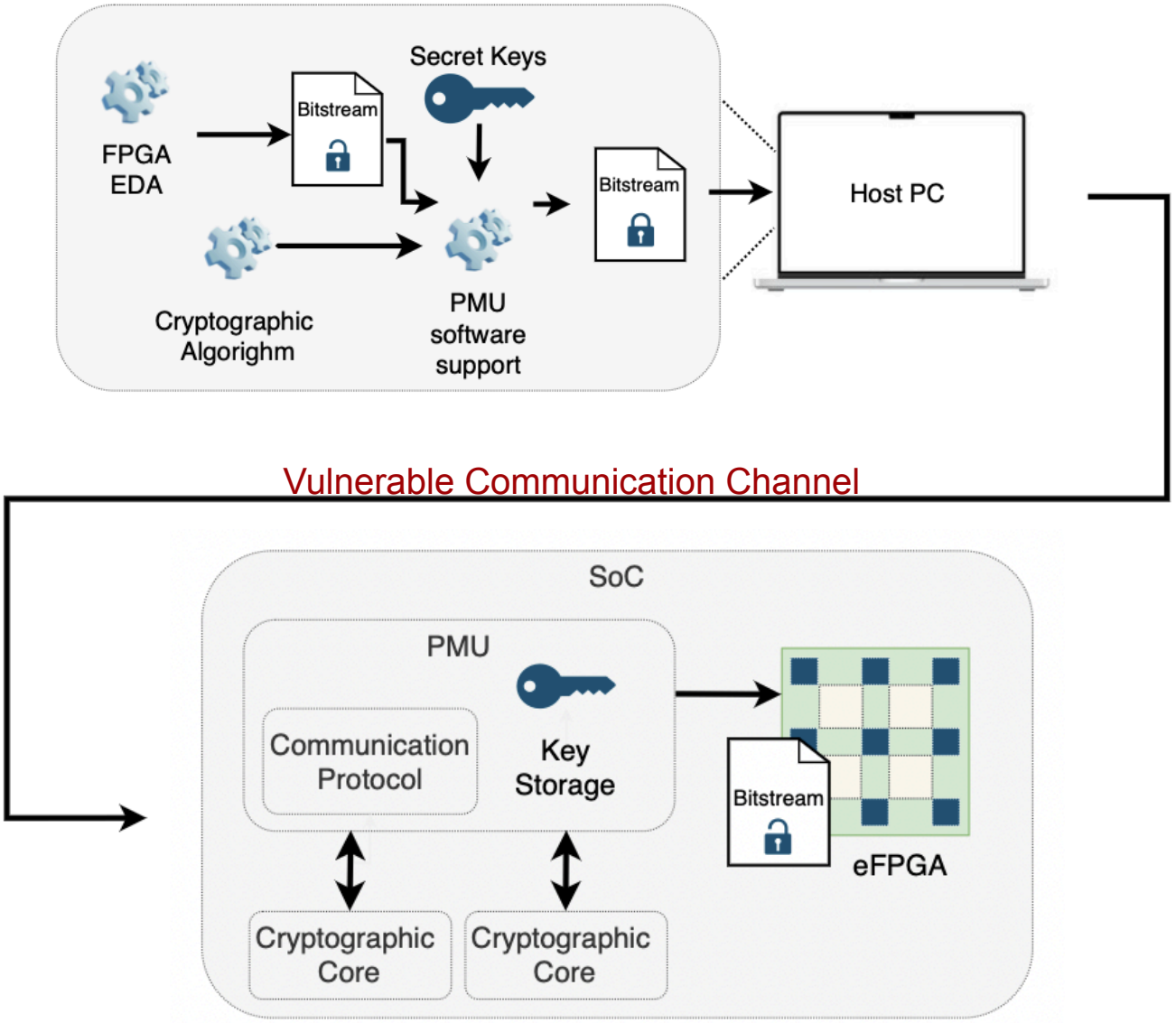

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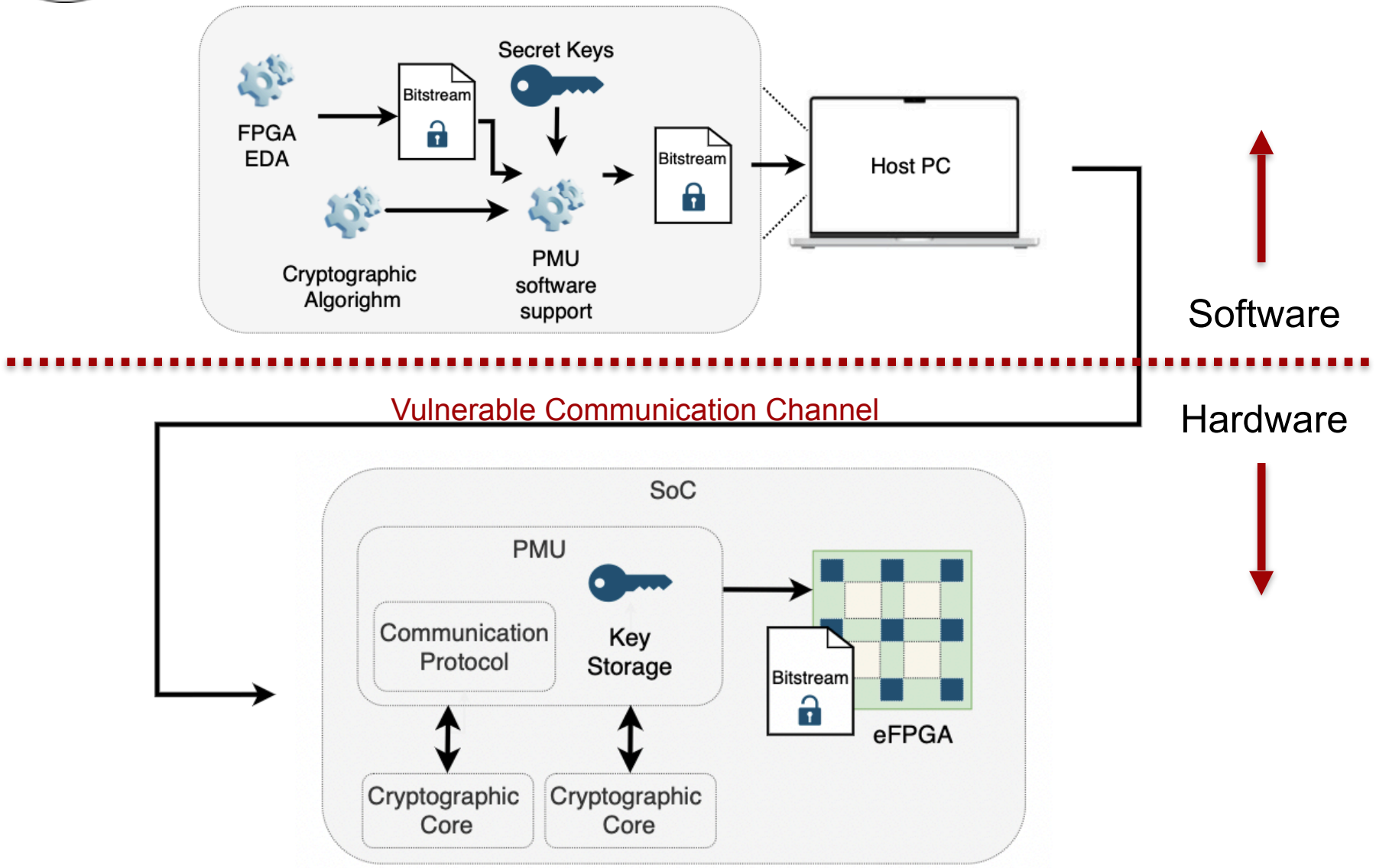

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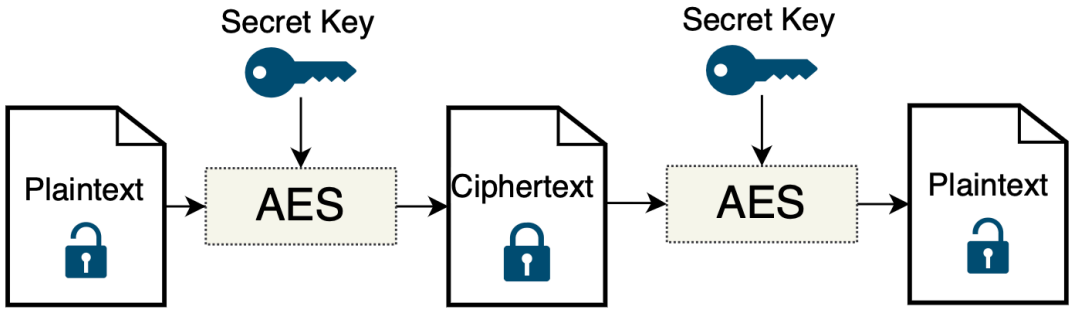

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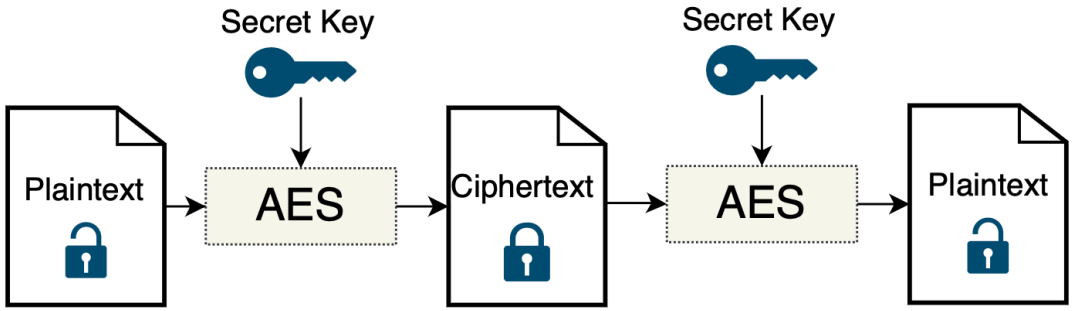

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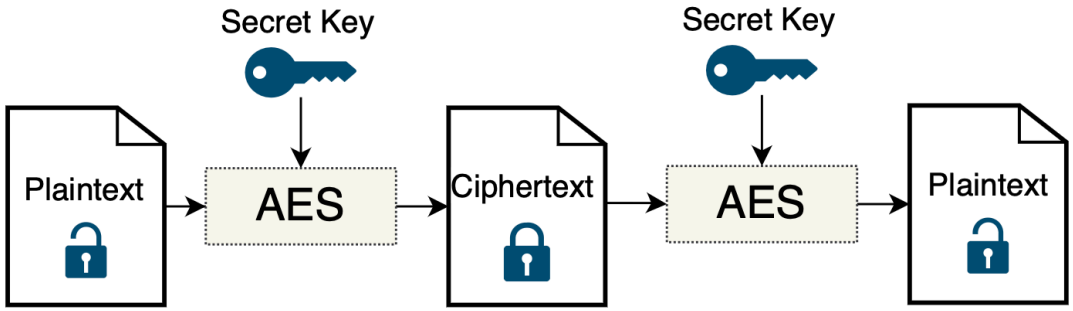

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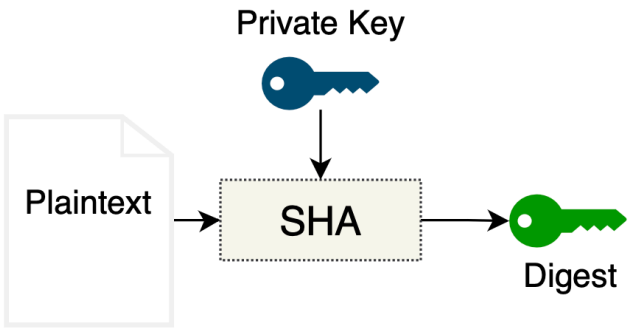
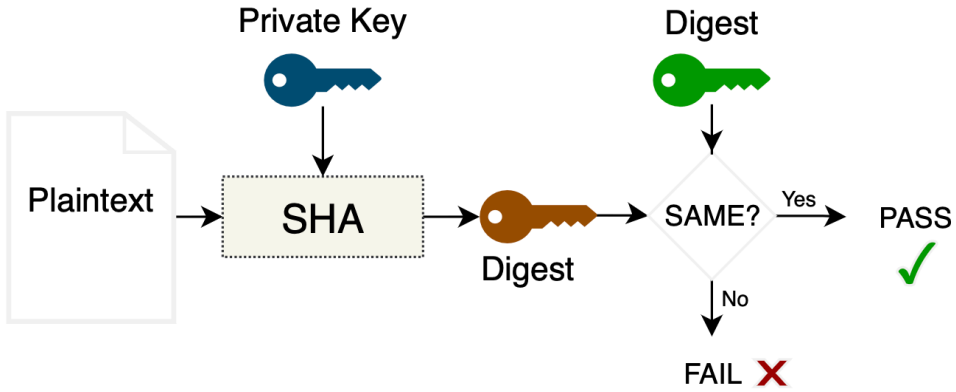
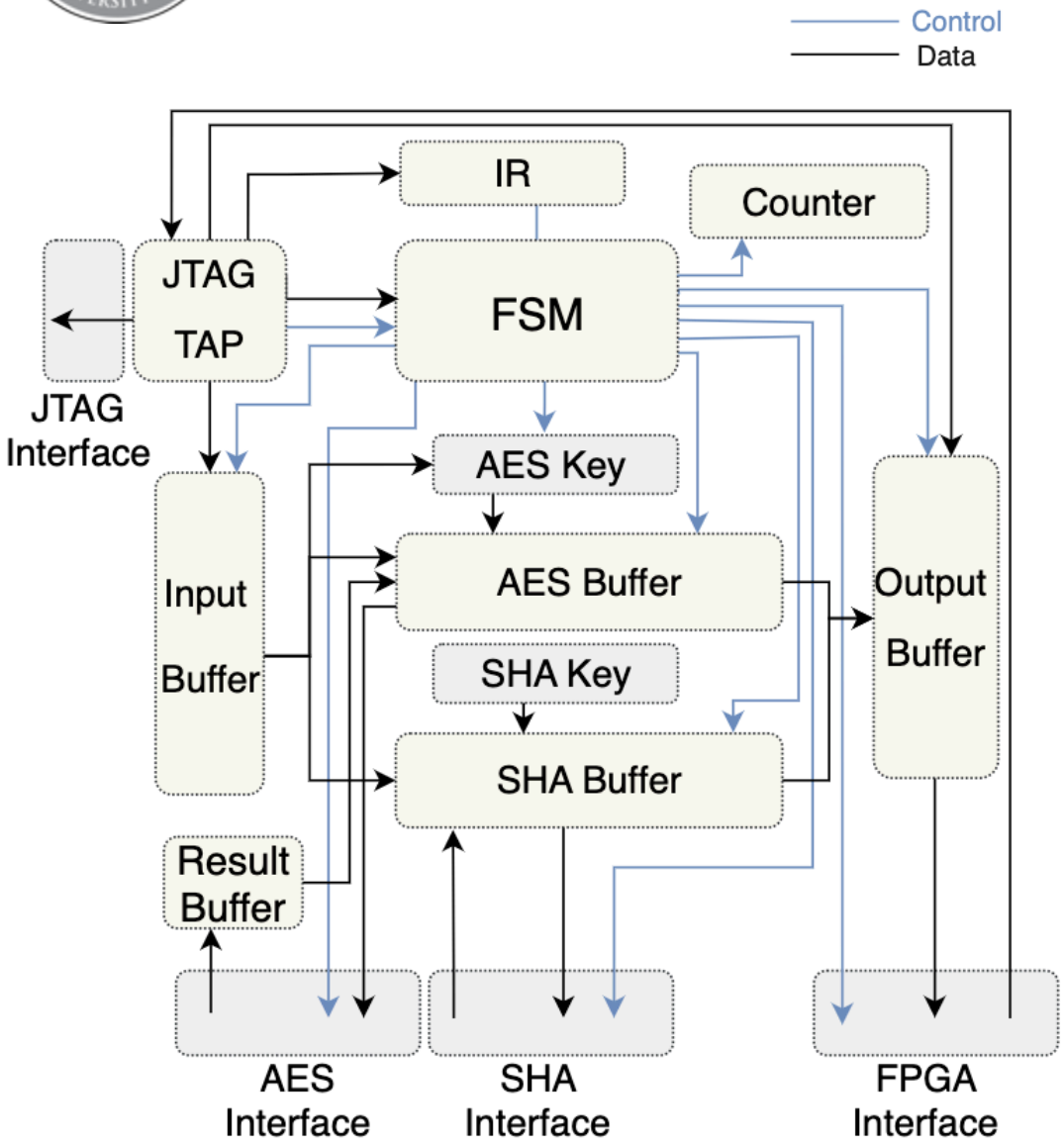




PMU Core Block Diagram



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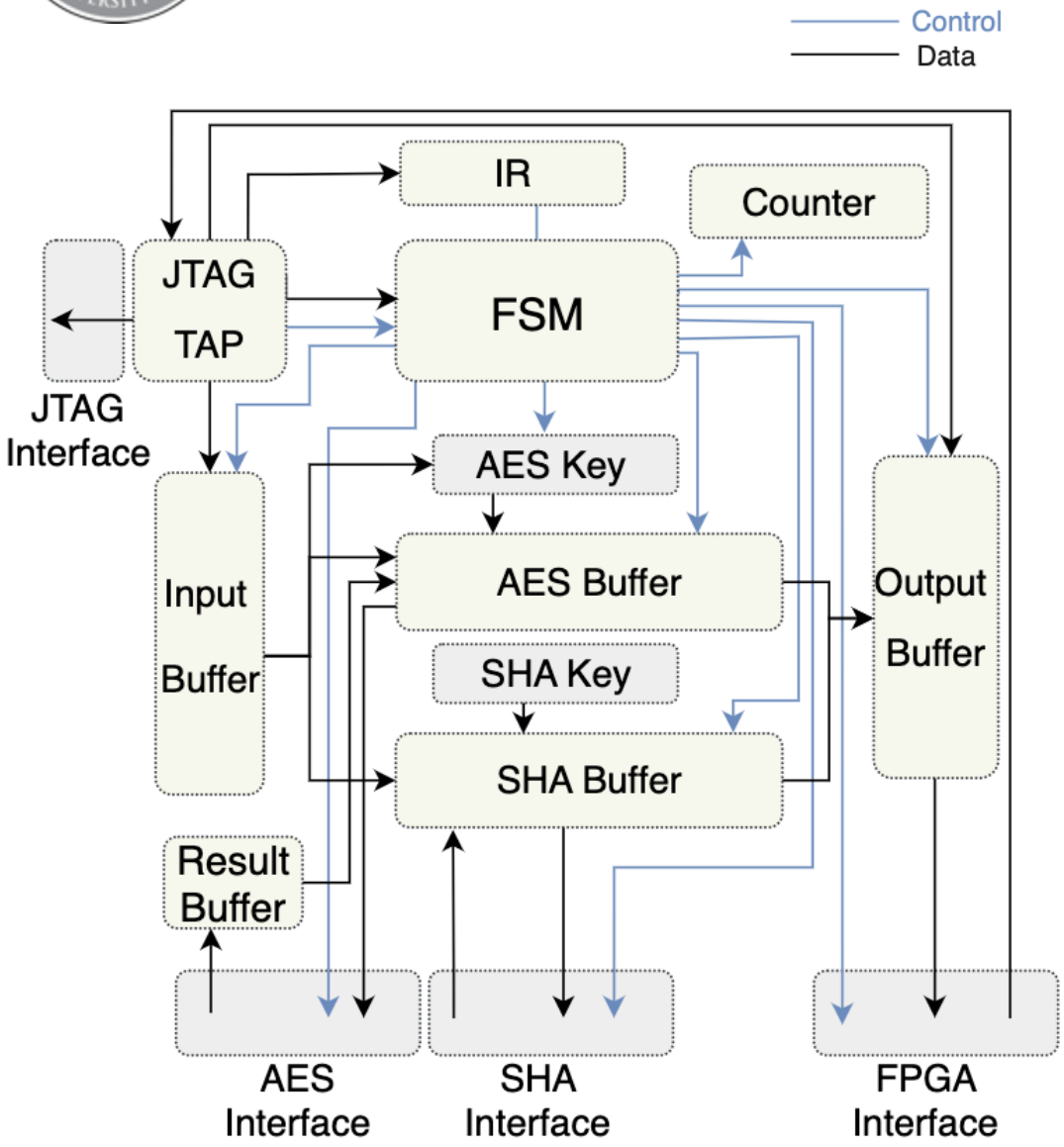

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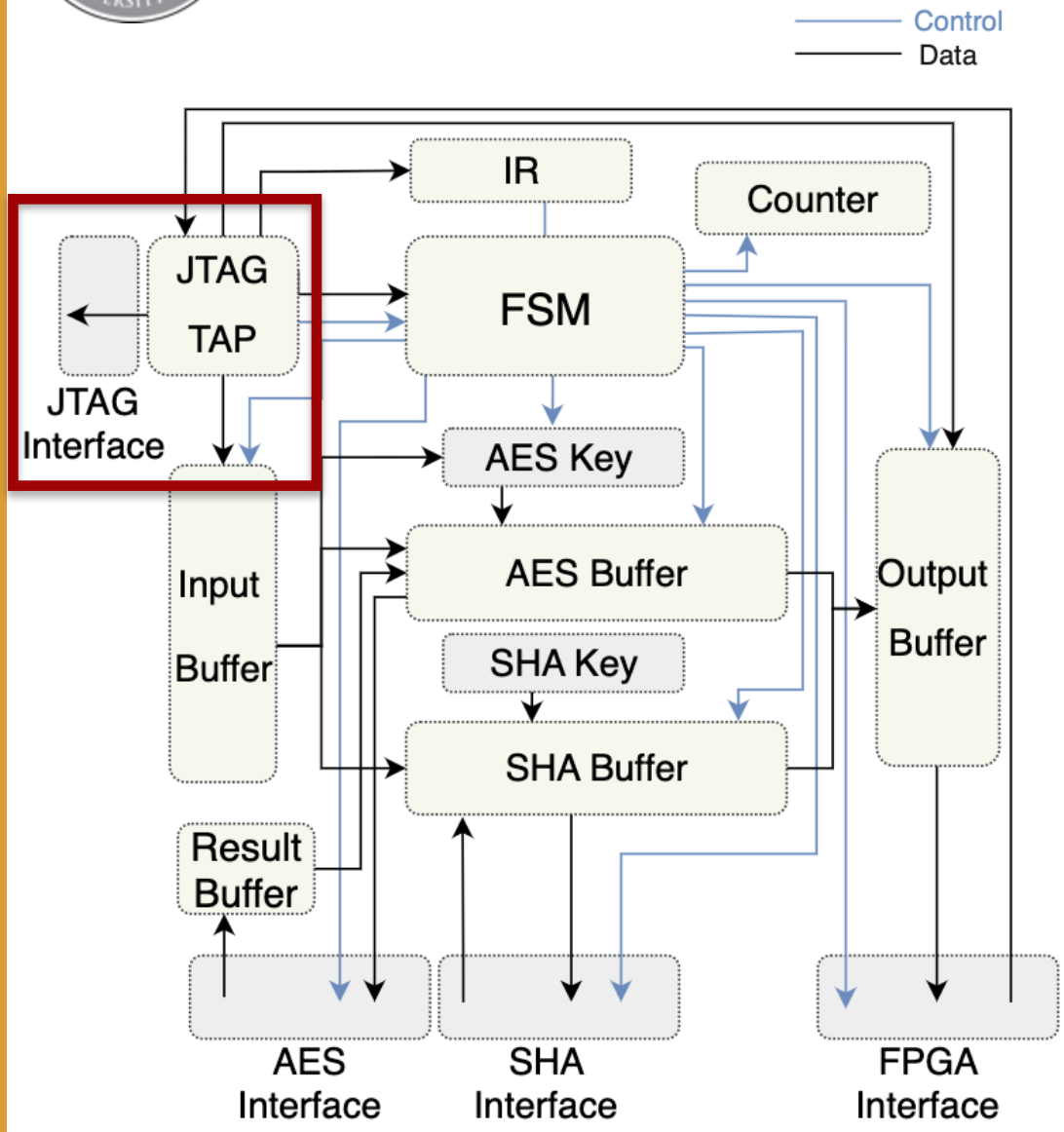

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  - SPI, I2C, USB

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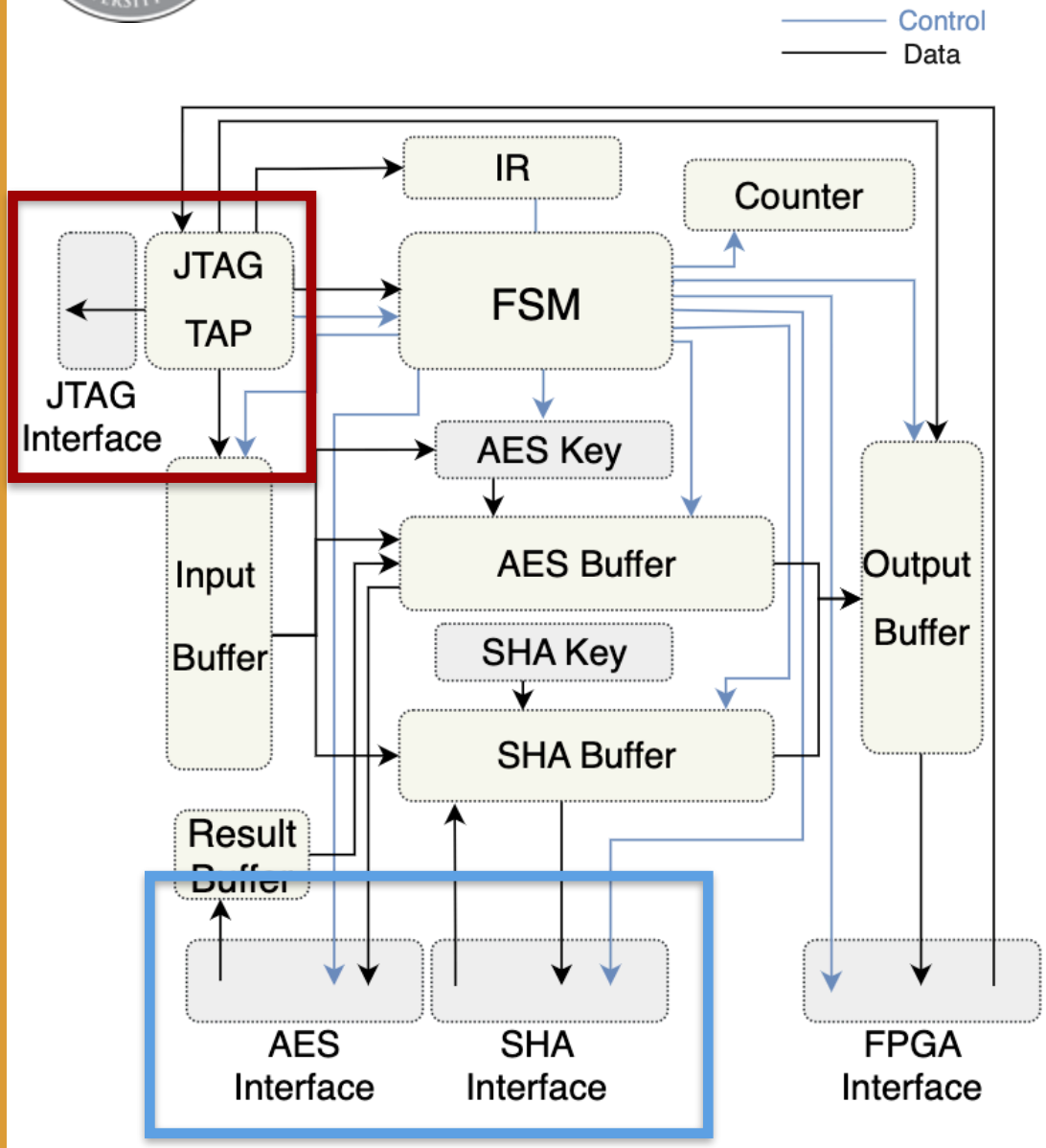

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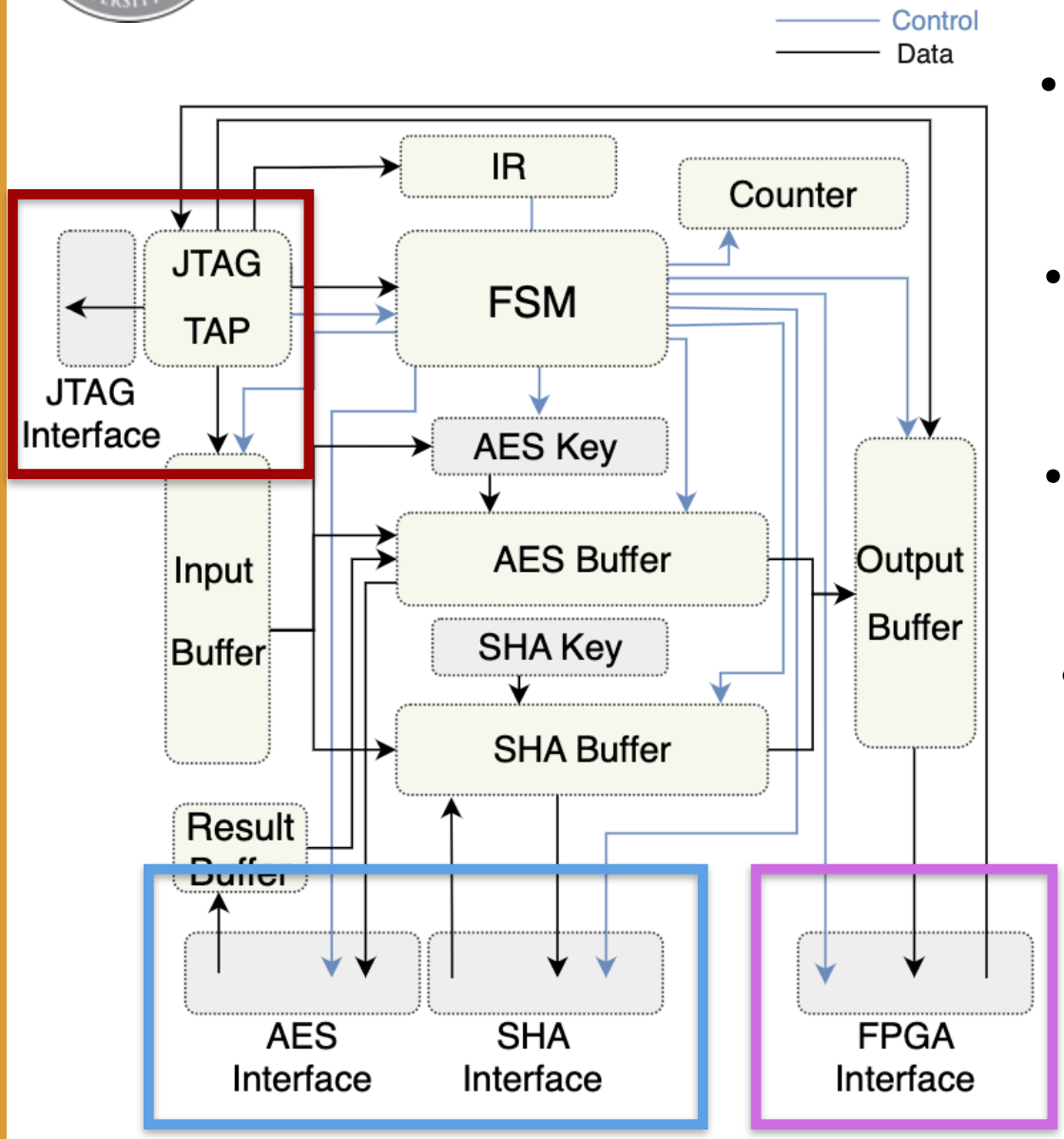

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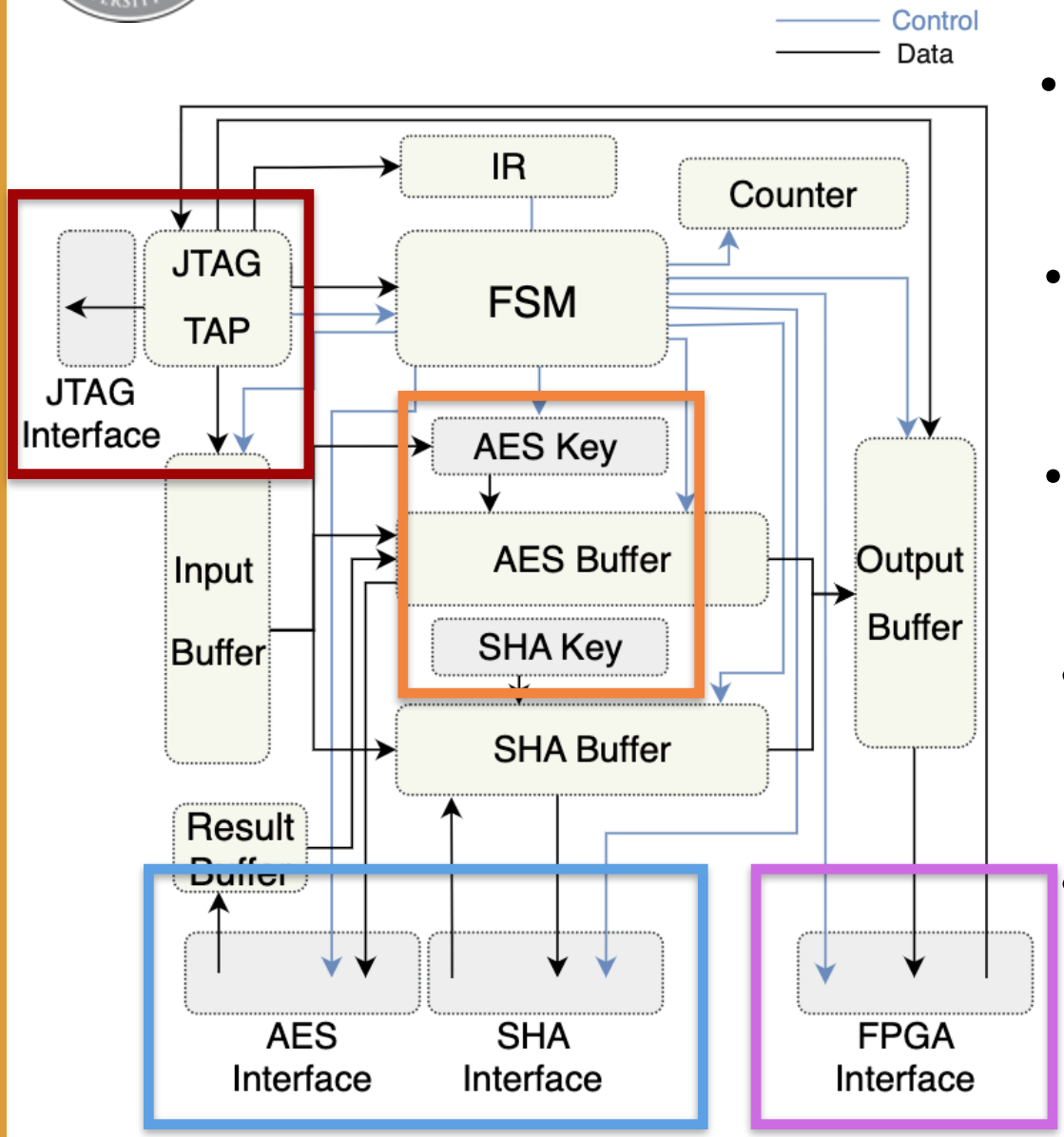

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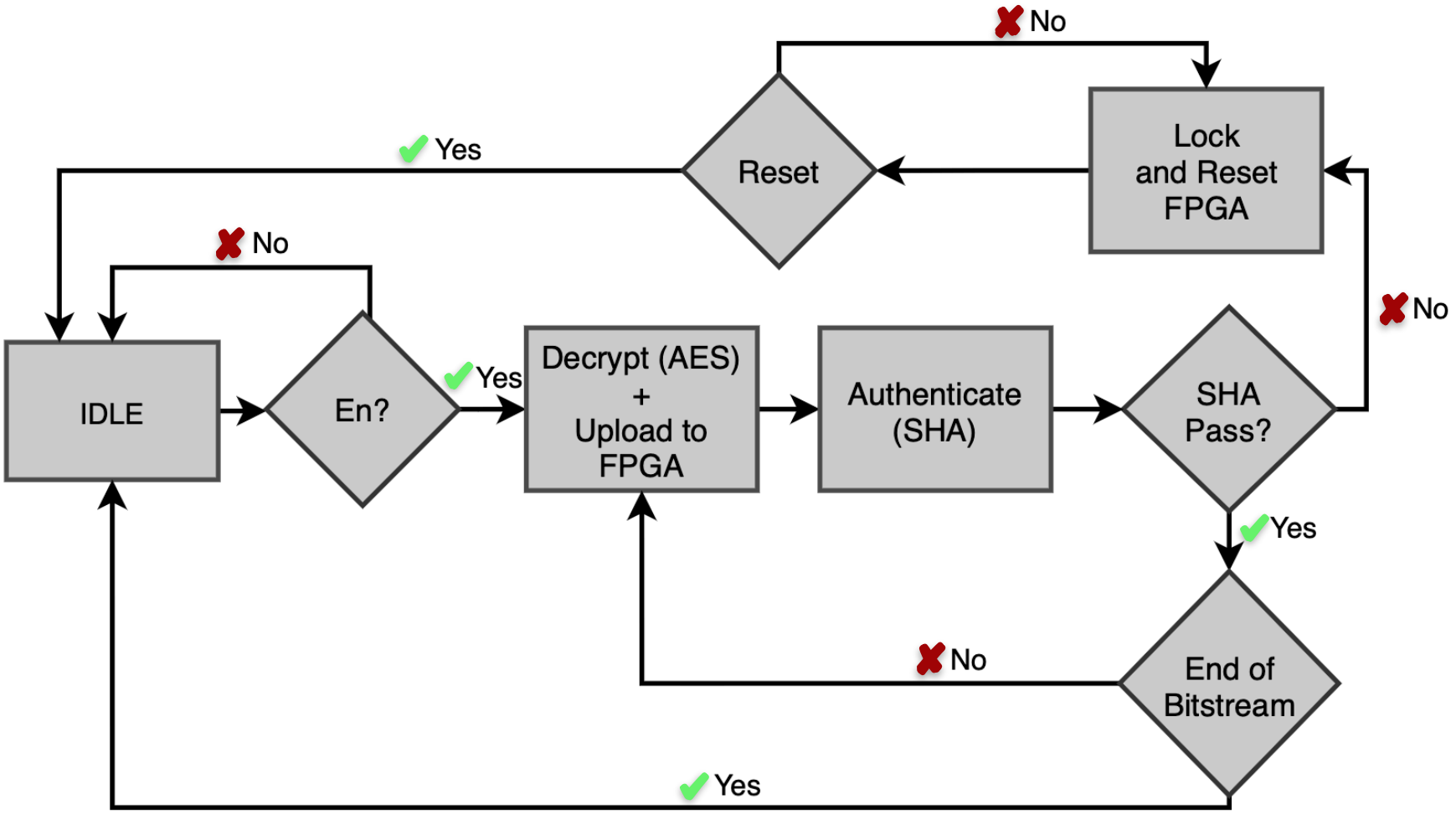
PMU Core Operation



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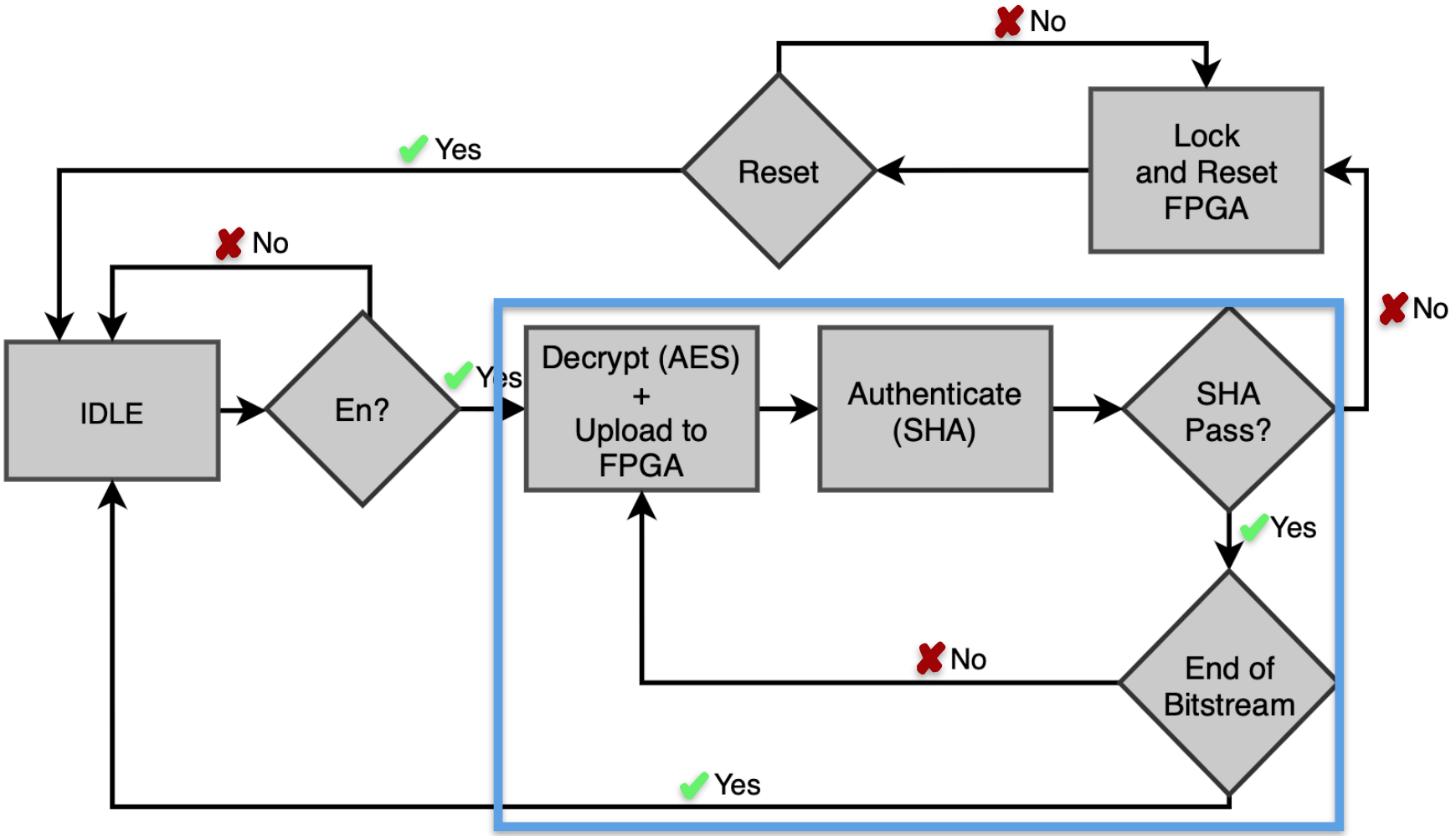

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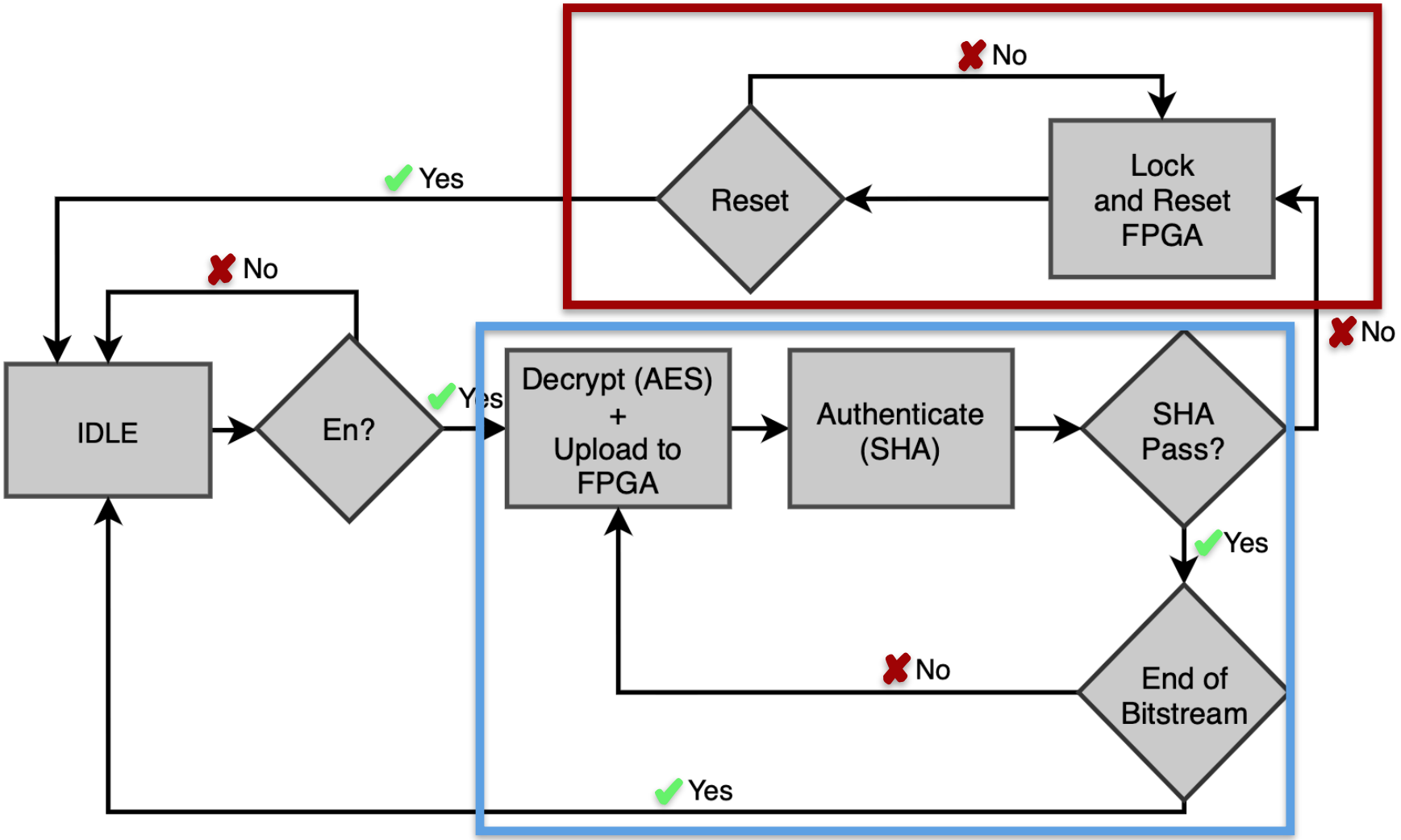

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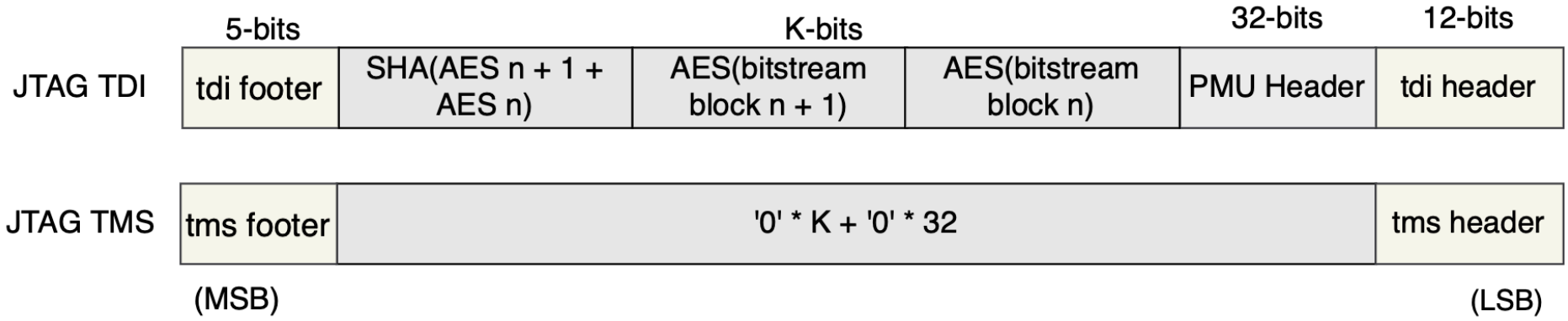

Encoding Scheme

	5-bits	K-bits		32-bits	12-bits
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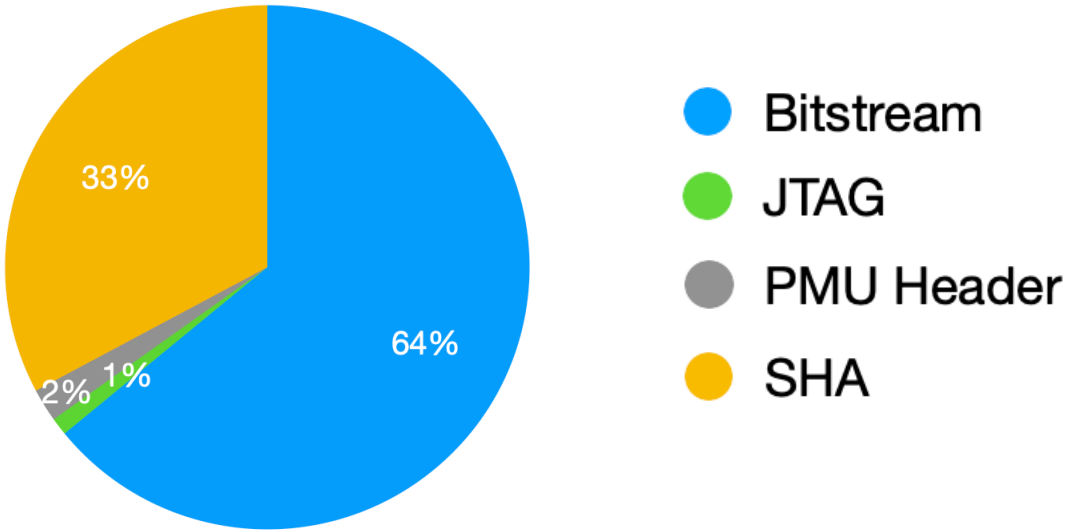
JTAG TMS	tms footer	'0' * K + '0' * 32	tms header

(MSB) (LSB)

- Consider 1000-bit bitstream
  - SHA evaluation every 500-bits



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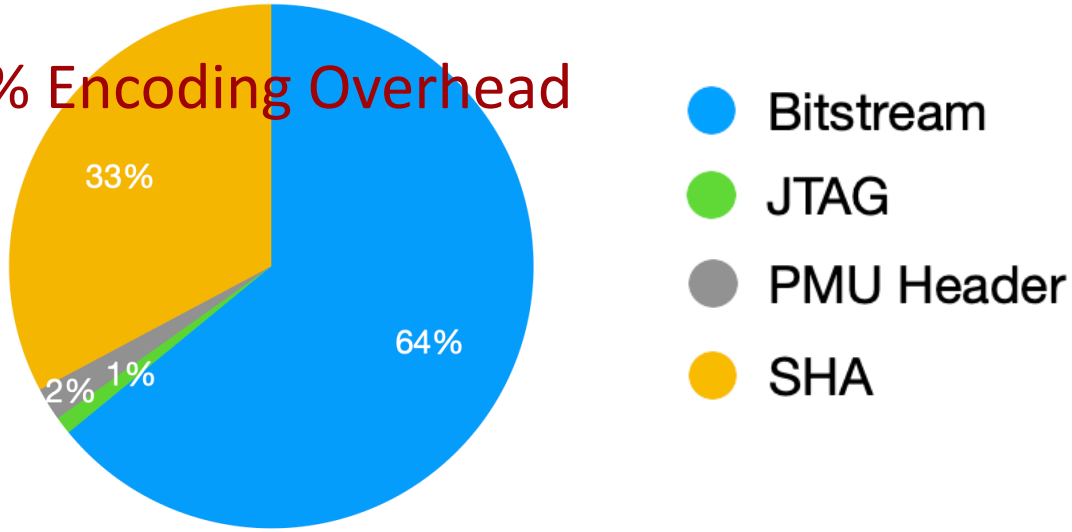

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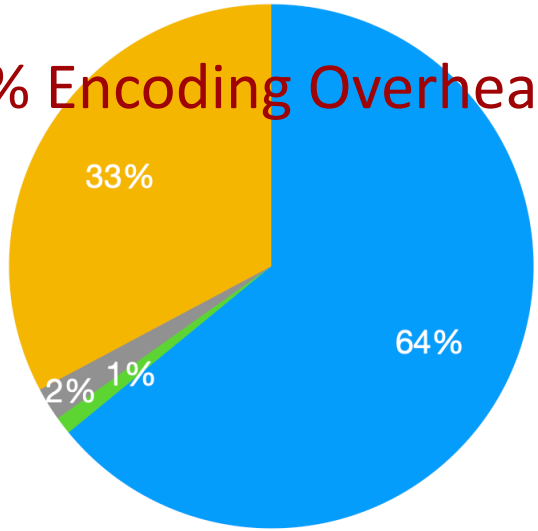

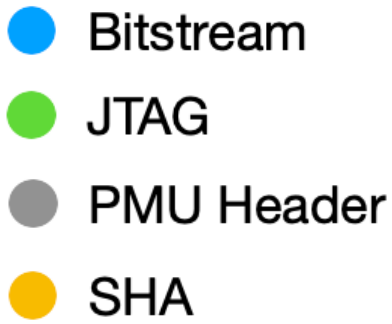

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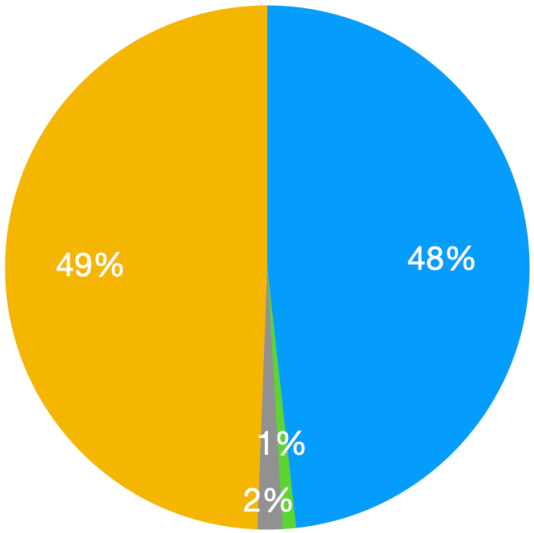

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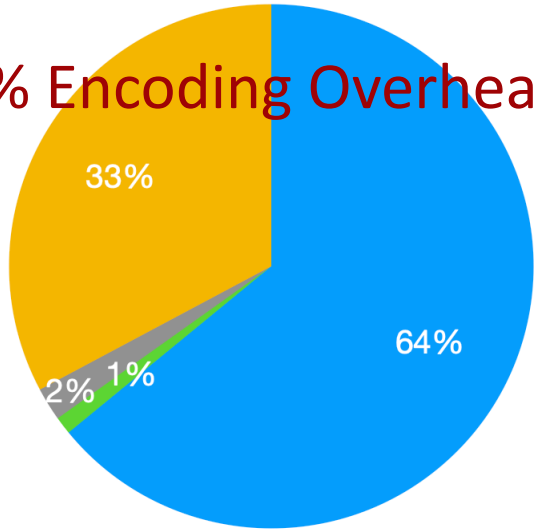

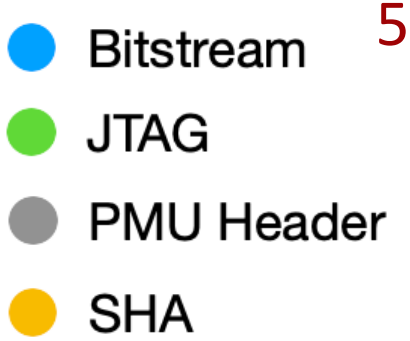

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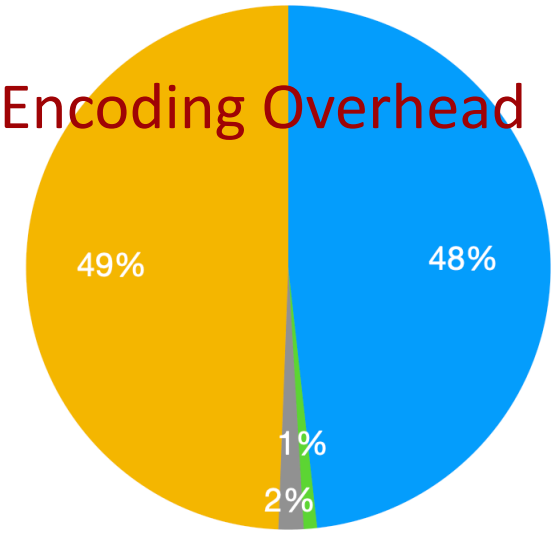
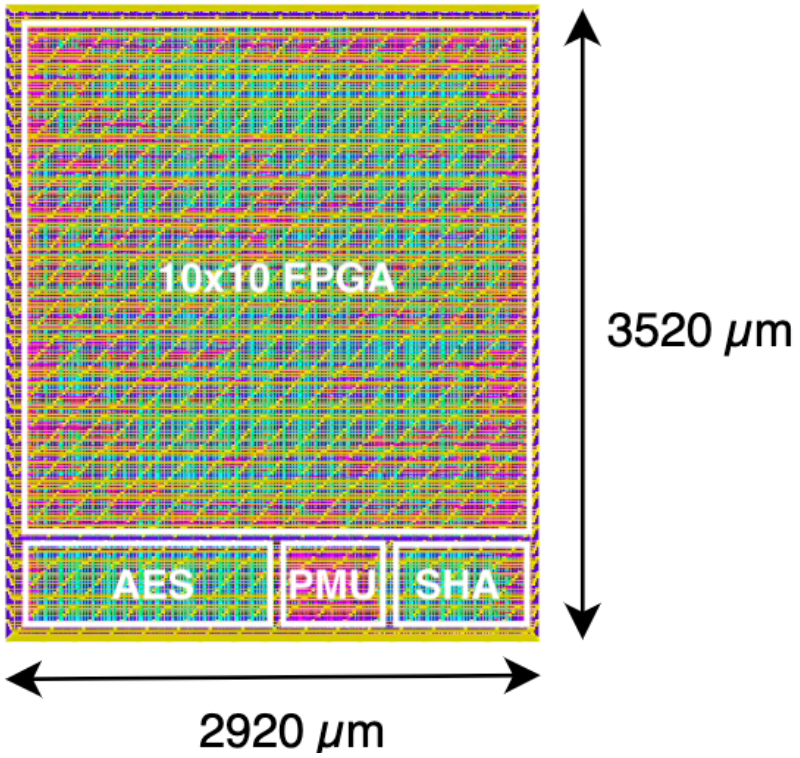


Silicon Integration to Caravel SoC



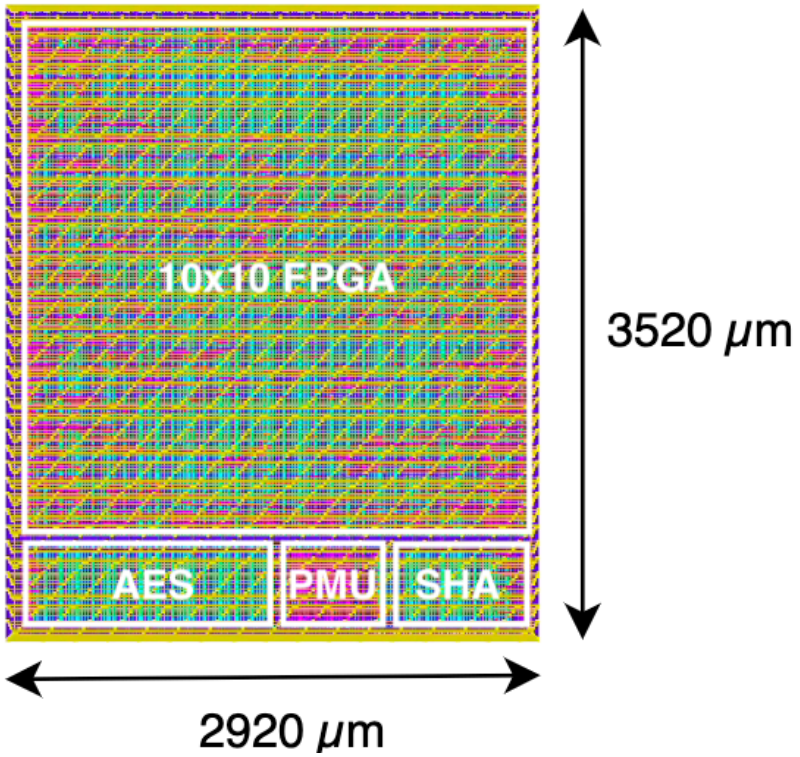
SiliconCompiler

Google + efabless.com

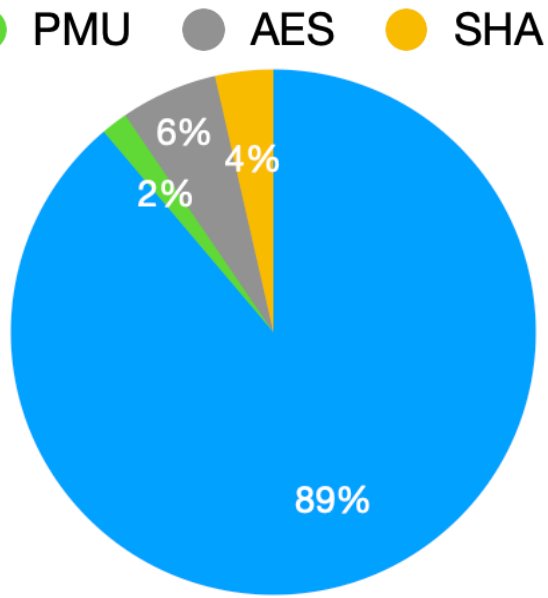
skywater TECHNOLOGY

PENFPGA

Silicon Integration to Caravel SoC



- Area (µm²)



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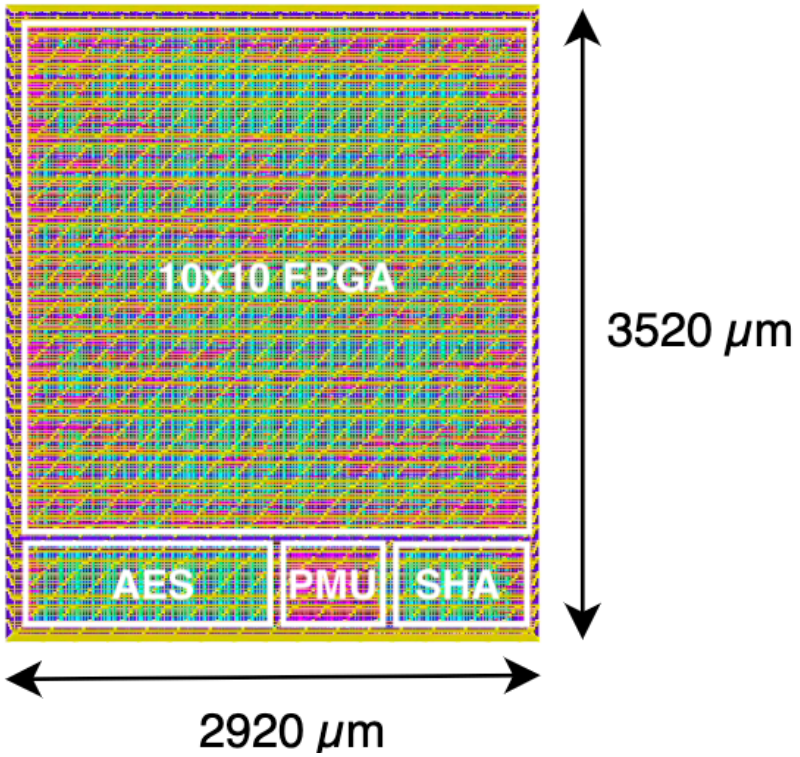
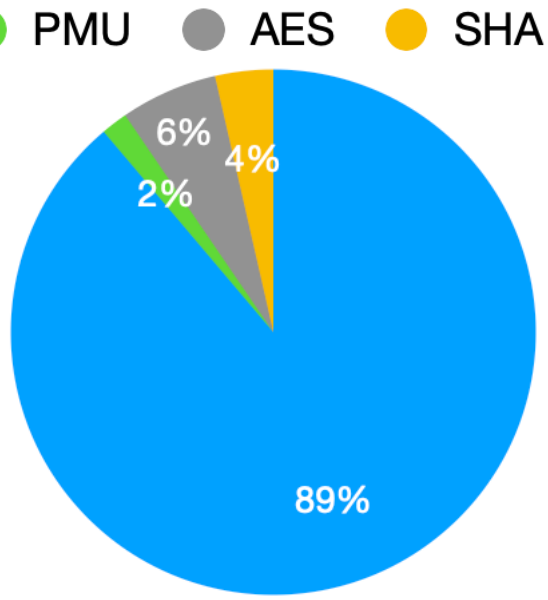
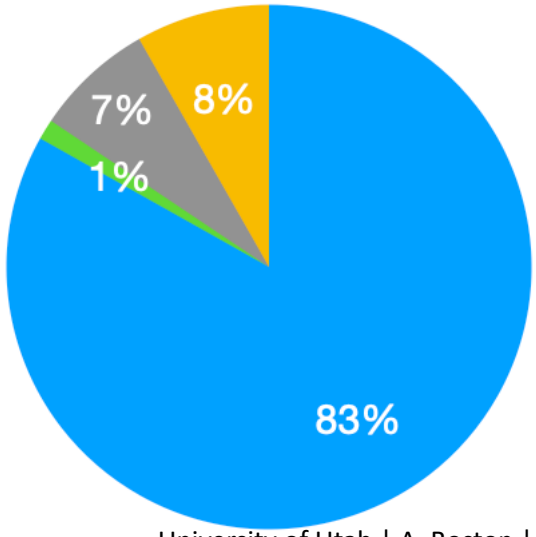


- Area (µm²)



- Power (W)



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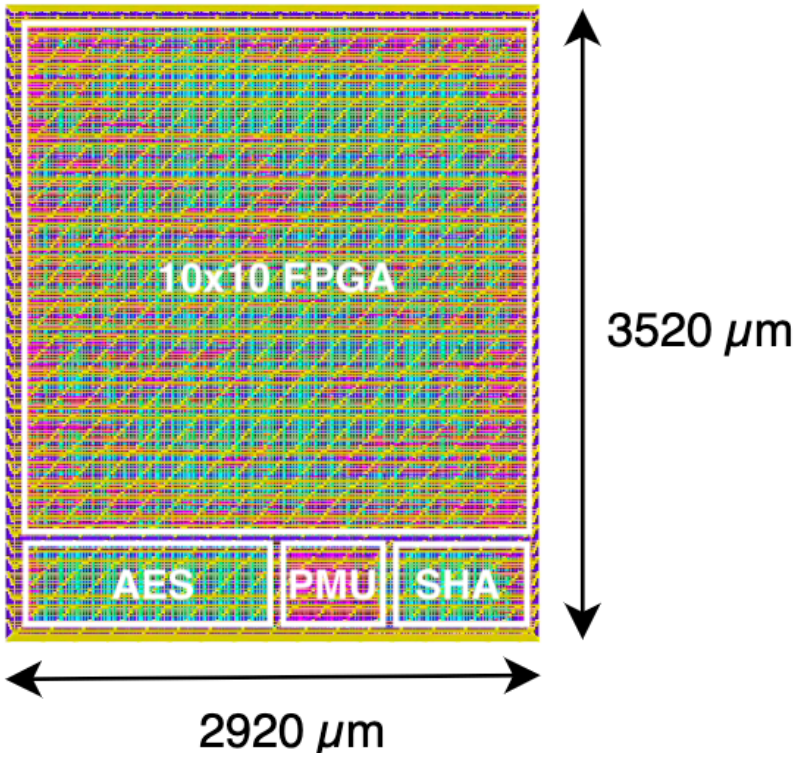
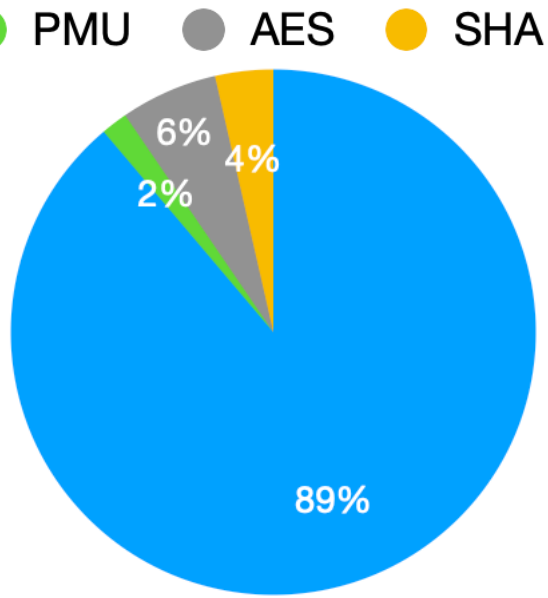


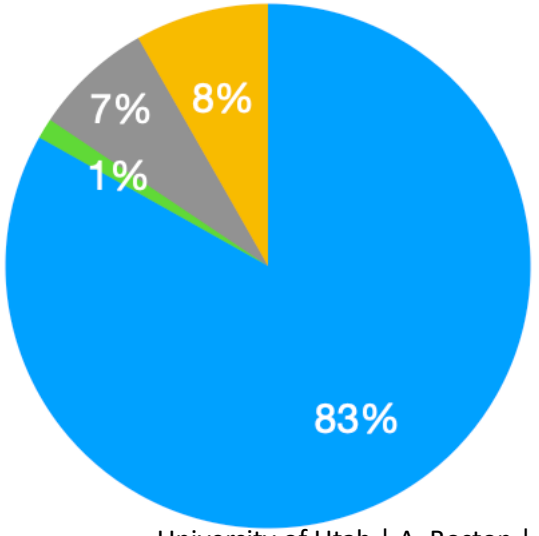
- Area (µm²)

12% Area Overhead



- Power (W)

16% Power Overhead



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PEN FPGA

Summary

- First open-source core specifically dedicated to FPGA configuration
- Flexible HW/SW template framework
- Enables secure and accurate FPGA configuration
- Demonstrated system integration utilizing open-source ecosystem

PMU Github:

https://github.com/lnis-uofu/FPGA_Secured_Bitstream

LNIS Laboratory for NanoIntegrated Systems

Thank you for your attention

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