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Open-Source FPGA on Silicon

Case Studies on PRGA

Ang Li, Ting-Jung Chang, Fei Gao, David Wentzlaff
Princeton University
angl@princeton.edu

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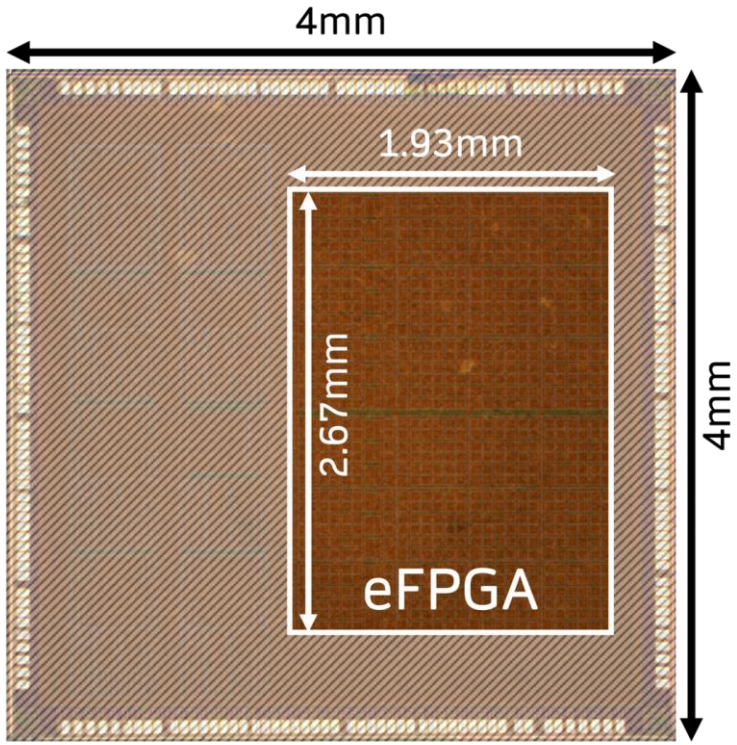
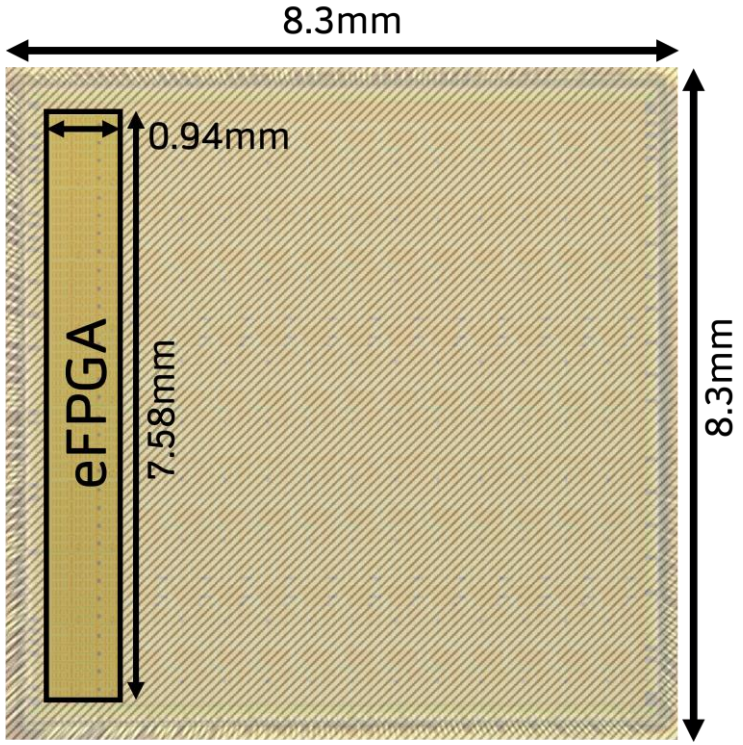


CIFER[1] eFPGA



DECADES[2] eFPGA

Open-Source Hardware | 12nm FinFET | Open-Source Software

7K BLEs | BRAM | DSP | Multi-Modal LUT6 | Carry Chain | Fast Configuration

1. T.-J. Chang*, A. Li*, F. Gao, T. Ta, G. Tziantzioulis, Y. Ou, M. Wang, J. Tu, K. Xu, P. Jackson, A. Ning, G. Chirkov, M. Orenes-Vera, S. Agwa, X. Yan, E. Tang, J. Balkind, C. Batten, and D. Wentzlaff, *"CIFER: A 12nm, 16mm2, 22-Core SoC with a 1541 LUT6/mm2, 1.92 MOPS/LUT, Fully Synthesizable, Cache-Coherent, Embedded FPGA"*, CICC'23
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FPGAs are increasingly being used …

For Open-Source Hardware Research & Prototyping

ESP

OpenPiton

CHIPYARD

In Long-Term Production Systems

- Project Catapult
- Project Brainwave

EC2 F1 Cloud FPGAs

aws

SAMSUNG

SmartSSD

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FPGAs are increasingly being used …

For Open-Source Hardware Research & Prototyping

In Long-Term Production Systems

Research on FPGAs themselves?
Silicon Prototyping of FPGAs?
Domain/Application-Specific FPGAs?

CHIPYARD

SAMSUNG

SmartSSD

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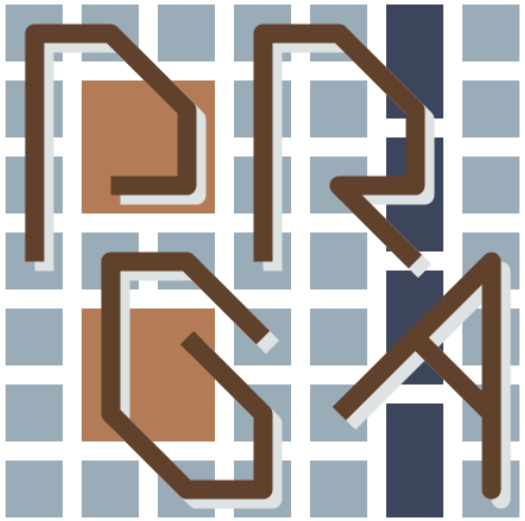

Princeton Reconfigurable Gate Array (PRGA)

An Open-Source FPGA Prototyping and Research Framework

Ang Li, David Wentzlaff, *"PRGA: An Open-Source FPGA Research and Prototyping Framework"*, FPGA'21

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- CIFER eFPGA & DECADES eFPGA
  - Architecture
  - Physical Design
- Evaluation
- Conclusion

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Princeton Reconfigurable Gate Array

- **Co-generation** of a custom FPGA and a bespoke CAD toolchain
  - Synthesizable: ASIC EDA + standard cells
  - Open-Source CAD: Yosys, VPR, FASM, iverilog, …

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  - Modern FPGA features: BRAM, DSP, multi-modal logic elements, …
  - Bring-your-own-modules

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  - Bring-your-own-modules
- Intuitive Python API
- Template-based, human-readable Verilog (Jinja)
- Automated simulation scripts at various levels of abstraction
- …

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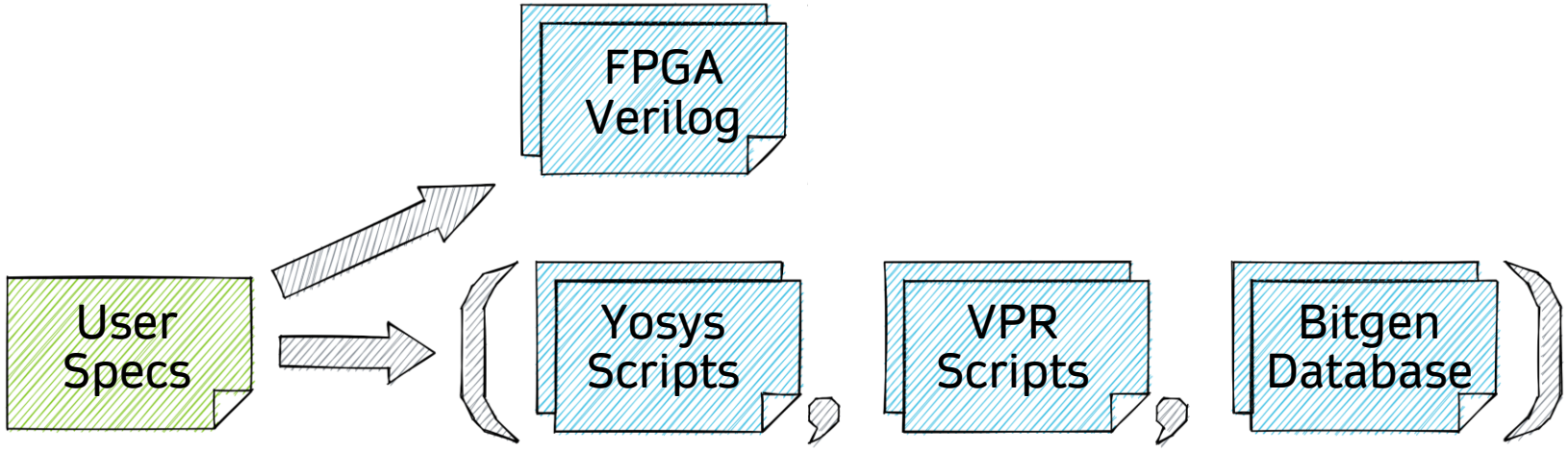
Princeton Reconfigurable Gate Array



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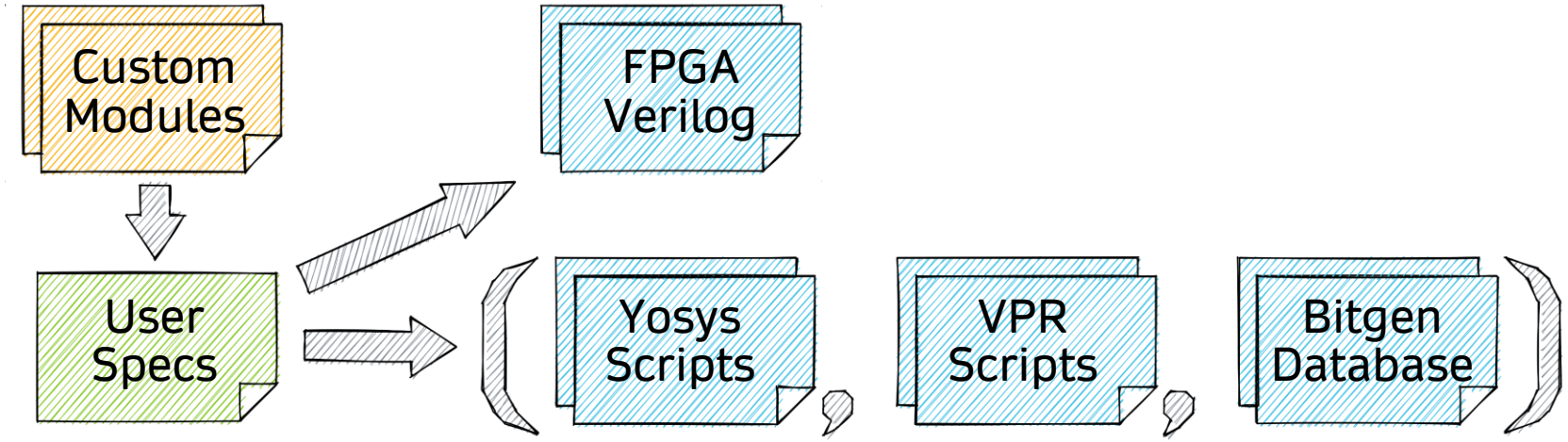

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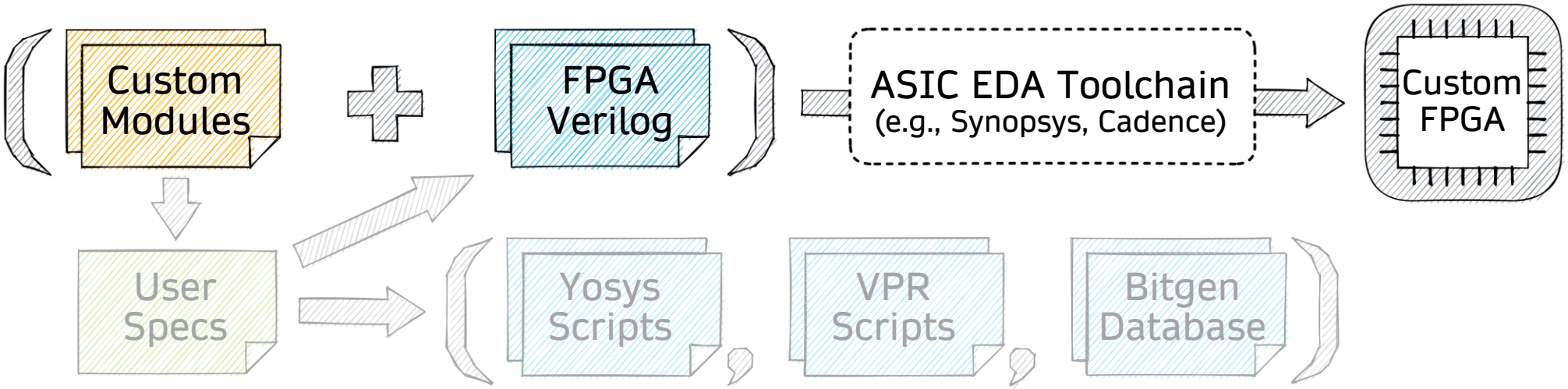

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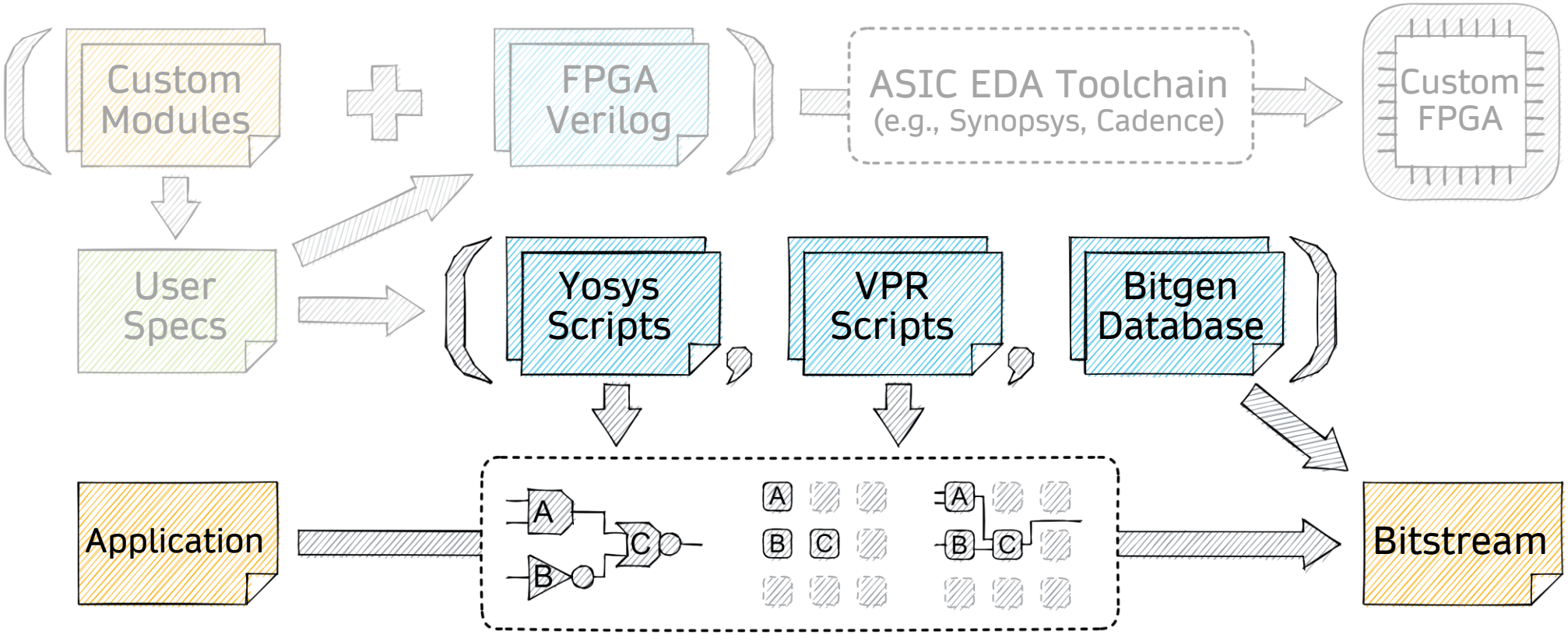

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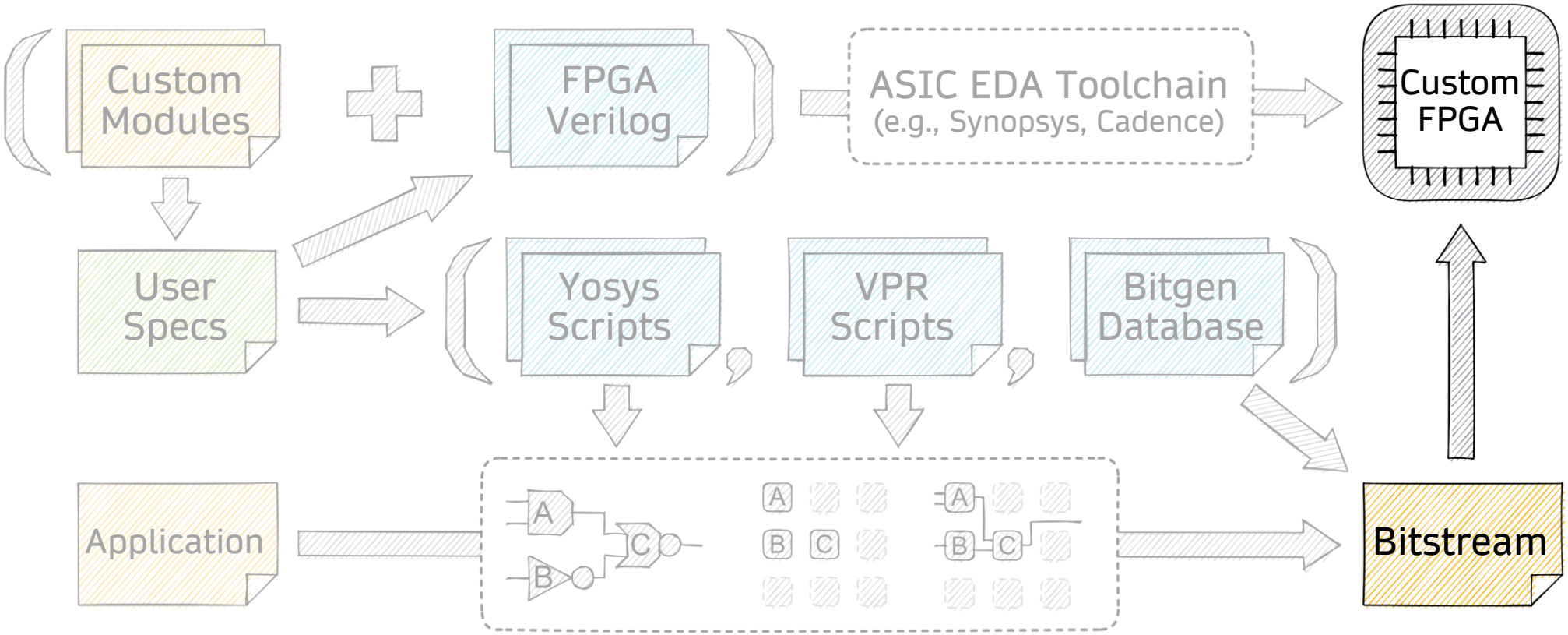

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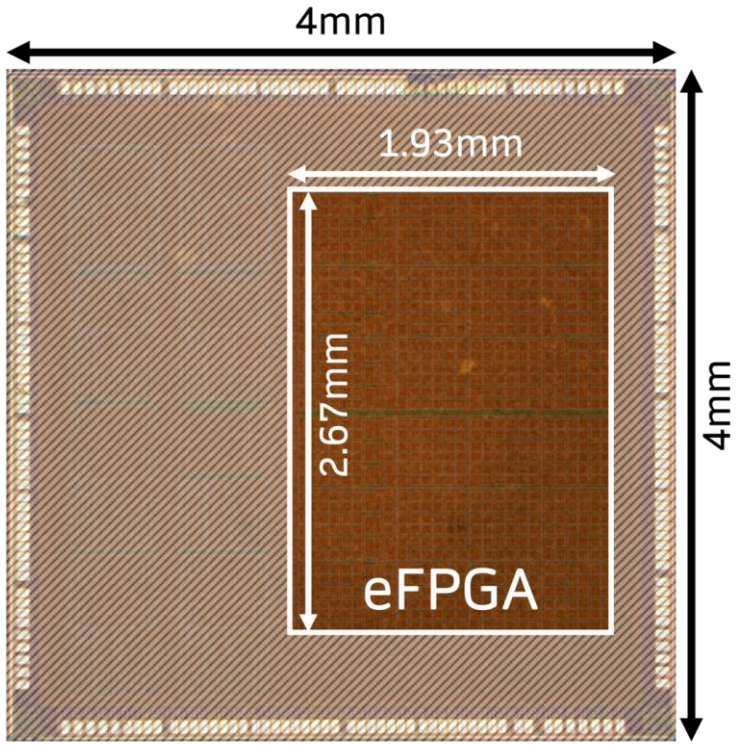

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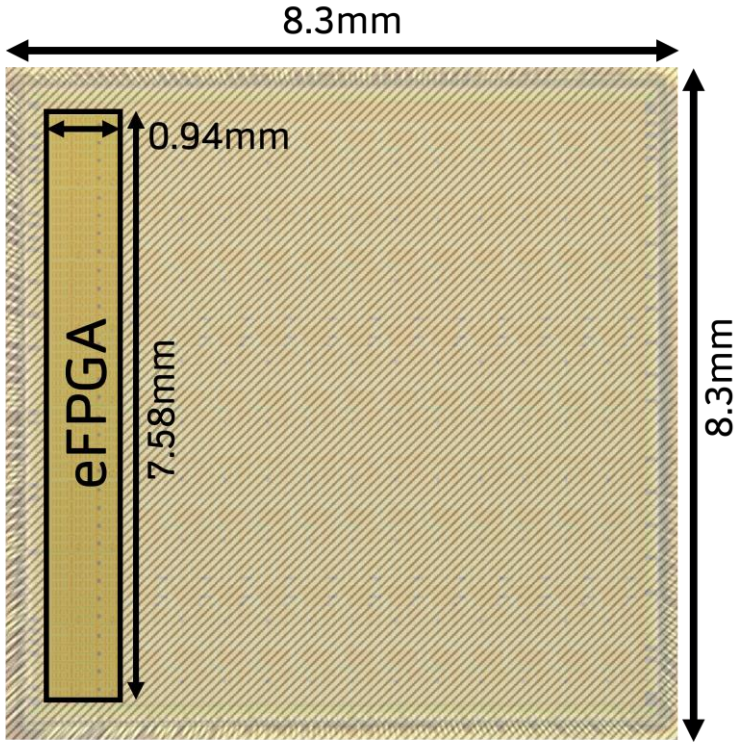

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Acknowledgements: CIFER Team


David Wentzlaff


Christopher Batten


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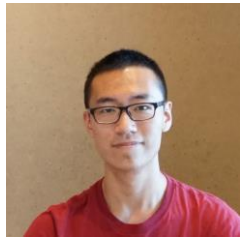
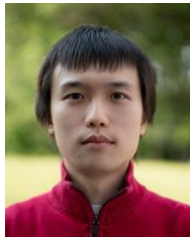
Ting-Jung Chang

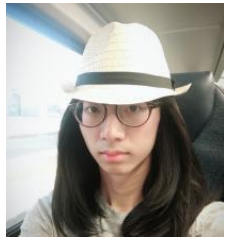

Fei Gao

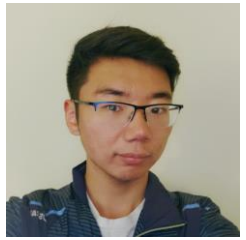

Tuan Ta


Georgios Tziantzioulis


Yanghui Ou


Moyang Wang


Jinzheng Tu


Kaifeng Xu


Paul Jackson


August Ning


Grigory Chirkov


Marcelo Orenes-Vera


Shady Agwa

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Cornell Engineering

& undergrads:
Xiaoyu Yan & Eric Tang

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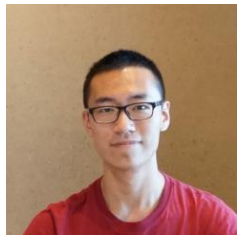
Acknowledgements: DECADES Team


David Wentzlaff


Luca Carloni


Margaret Martonosi


Jonathan Balkind


Fei Gao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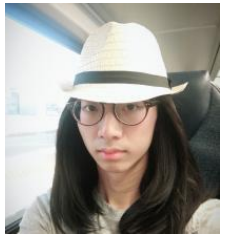
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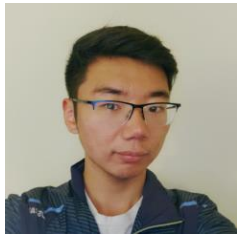
Kaifeng Xu


Grigory Chirkov


Gabriele Tombesi

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The Fu Foundation School of Engineering and Applied Science

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Architecture Overview

		CIFER eFPGA	DECADES eFPGA
Logic Resources	BLE (LUT6 + other)	6,720	7,040
	Routing Channel	160 (20× L1 + 15× L4)	200 (20× L1 + 20× L4)
	Block RAM	432Kb (18× 24Kb)	512Kb (32× 16Kb)
	Hard Multiplier	-	32× INT40
Configuration	Bitstream Size	~168KB	~192KB
	Config. Network	8-bit packet-switched + 1-bit shift-register	

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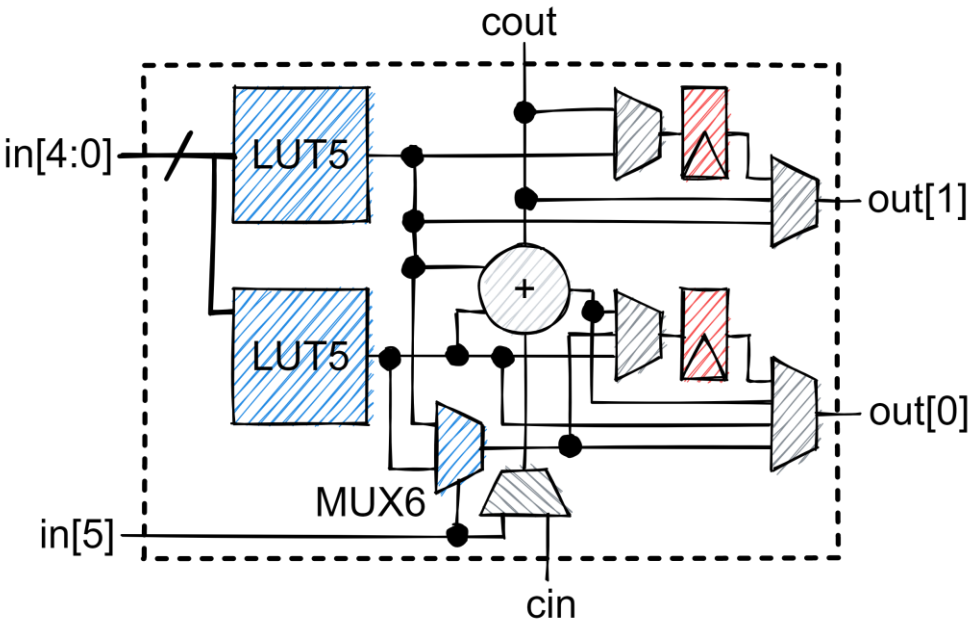
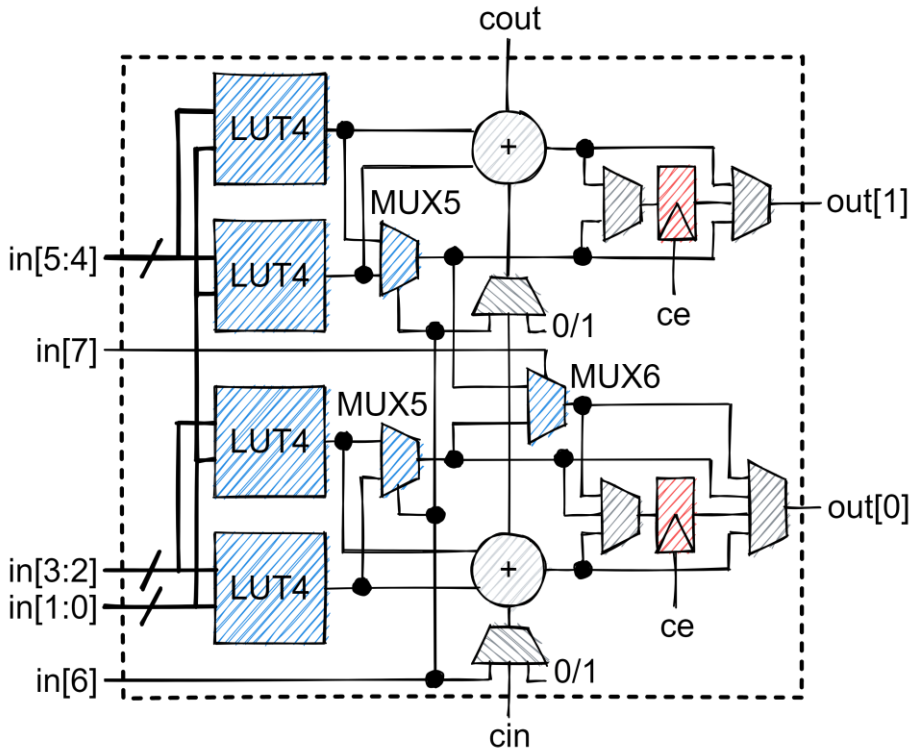
Basic Logic Element (BLE)

CIFER eFPGA BLE



DECADES eFPGA BLE



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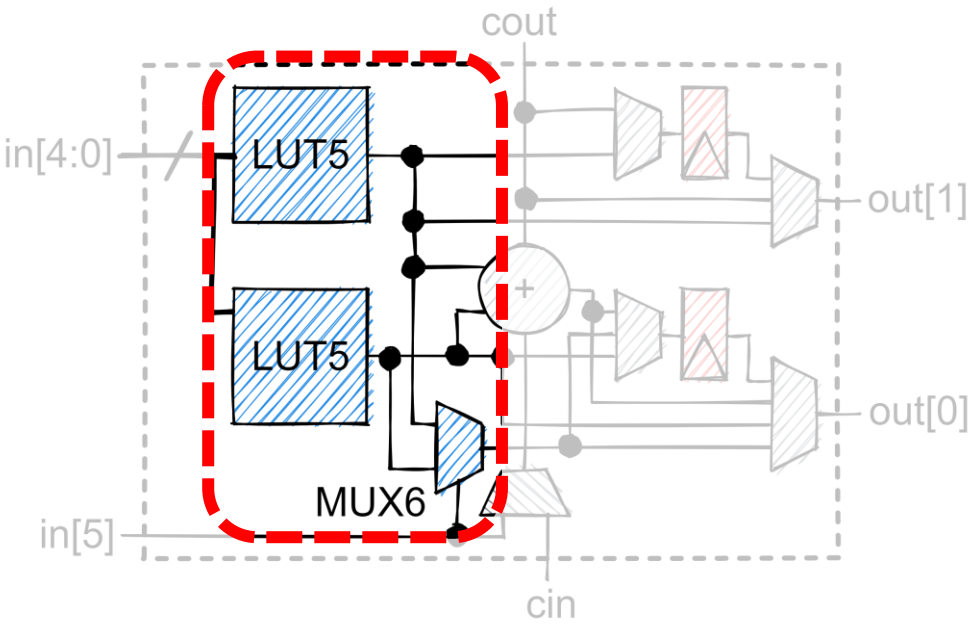
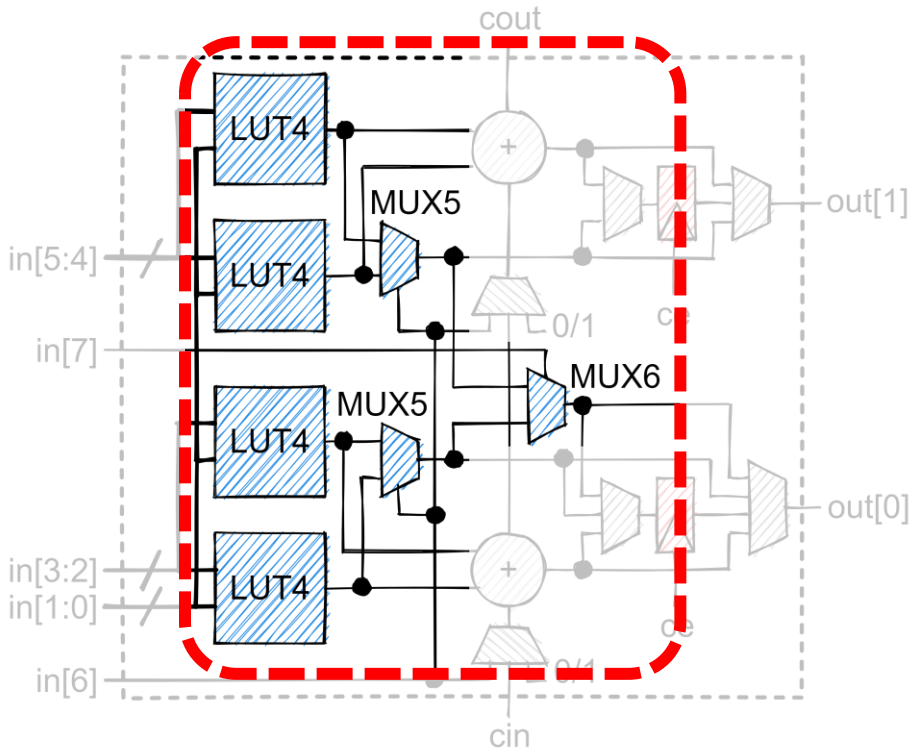


DECADES eFPGA BLE



Fracturable LUT

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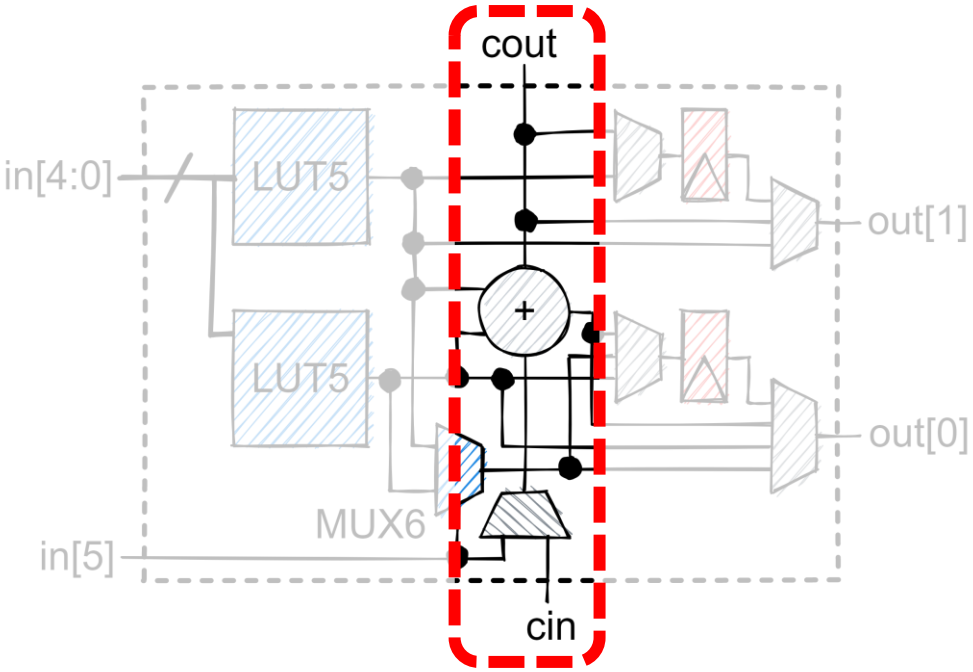
Basic Logic Element (BLE)

CIFER eFPGA BLE



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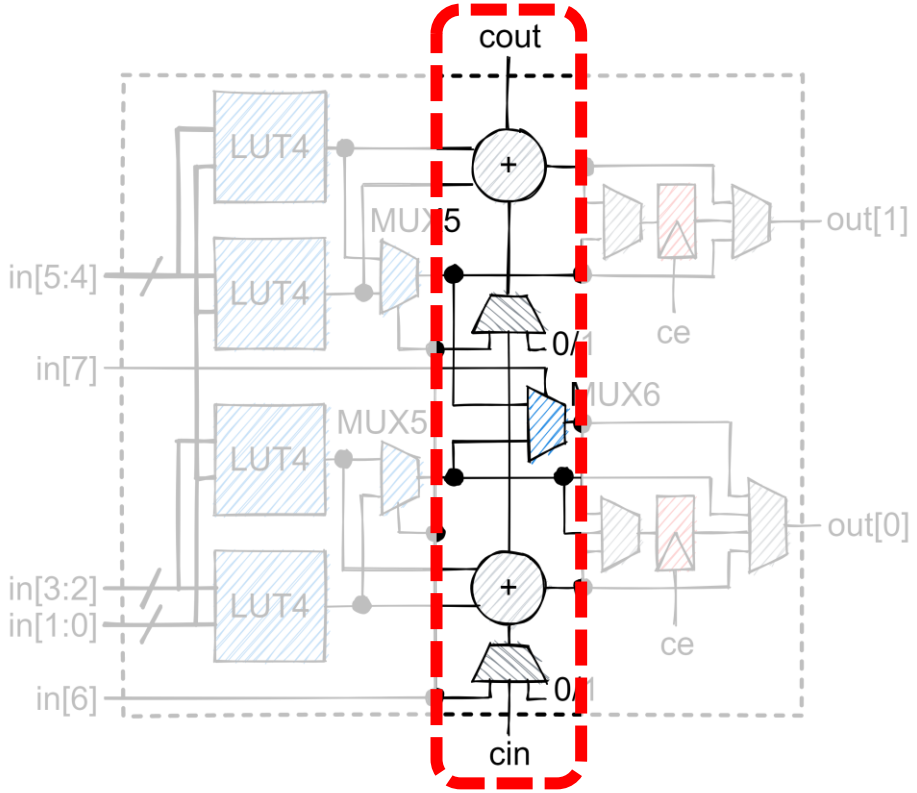

Fast Adder/Carry Chain

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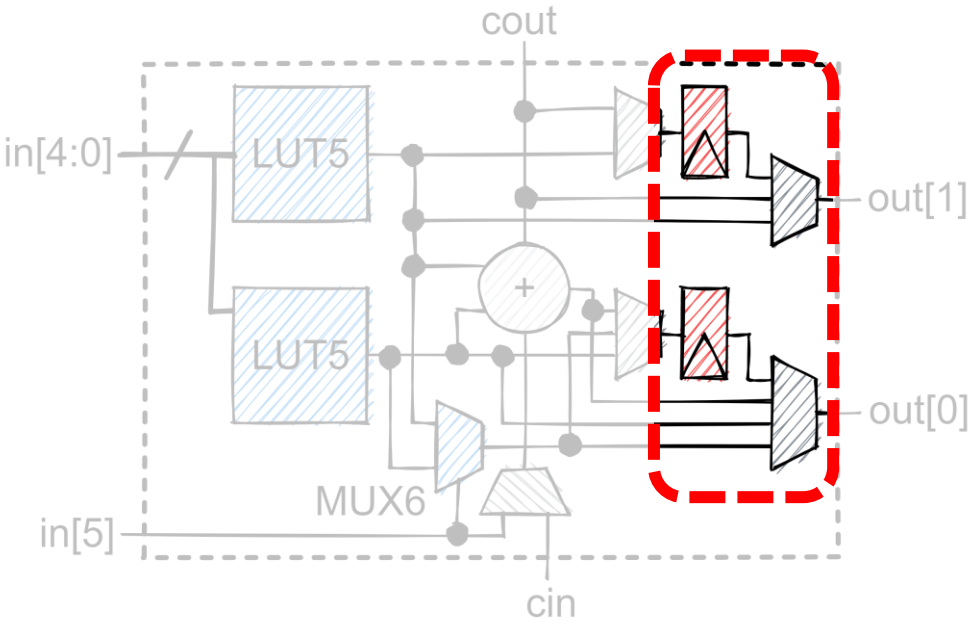

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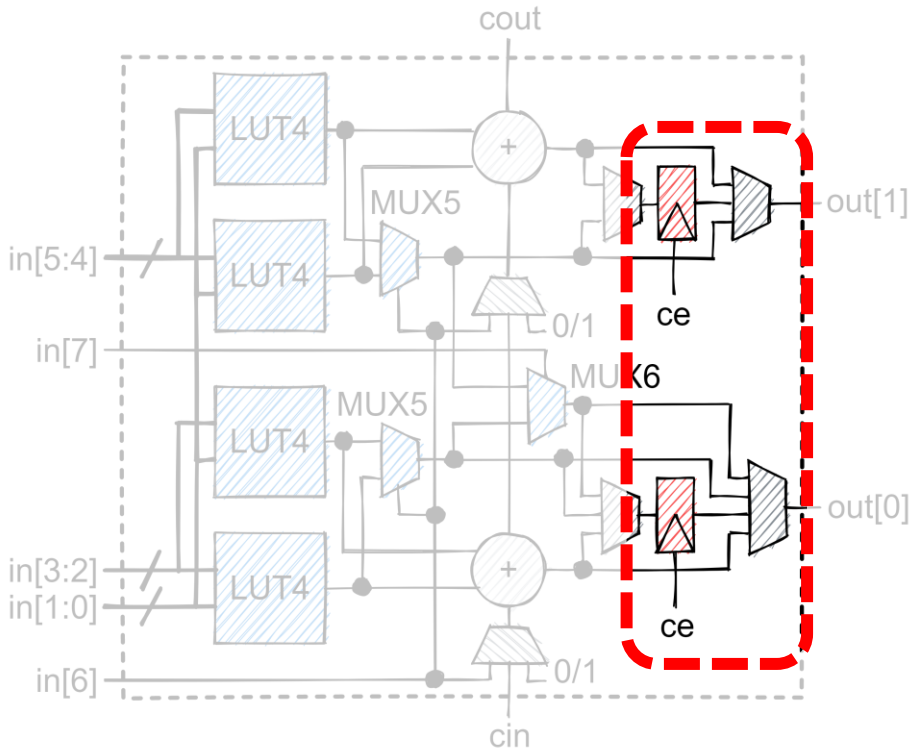

Bypass-able Registers

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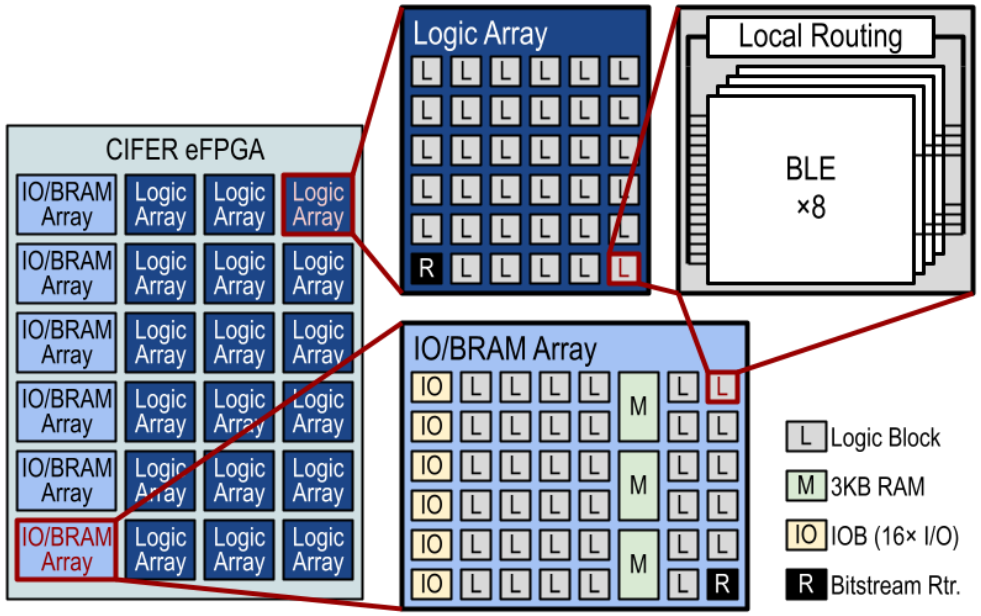
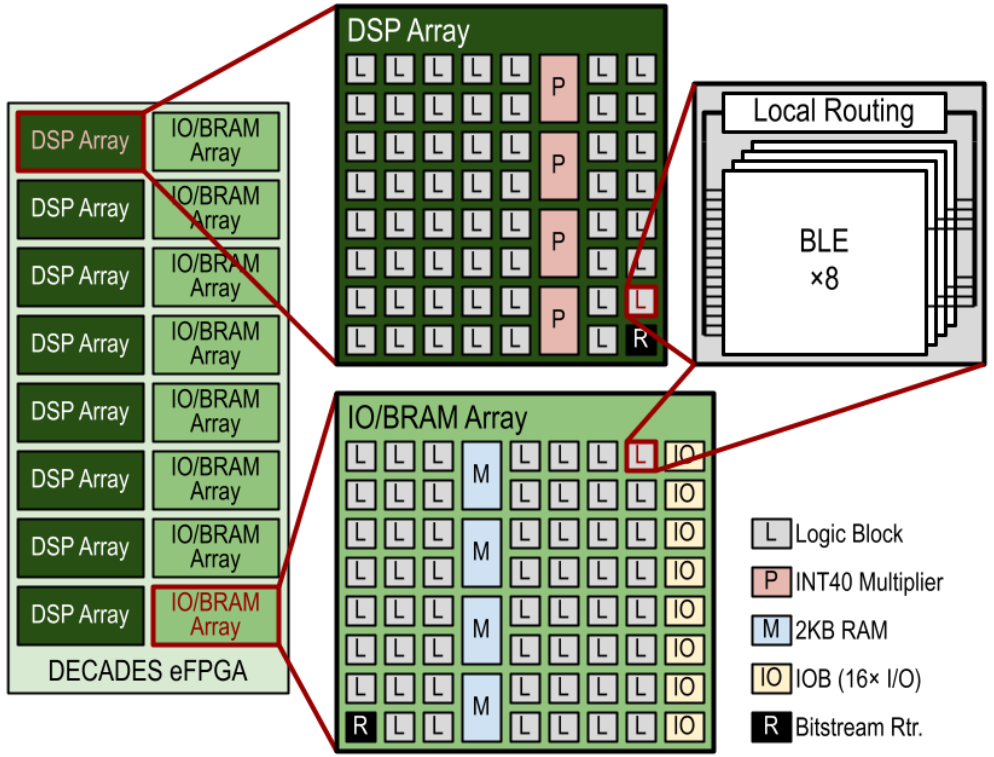
Hierarchical Design

CIFER eFPGA Hierarchy



DECADES eFPGA Hierarchy



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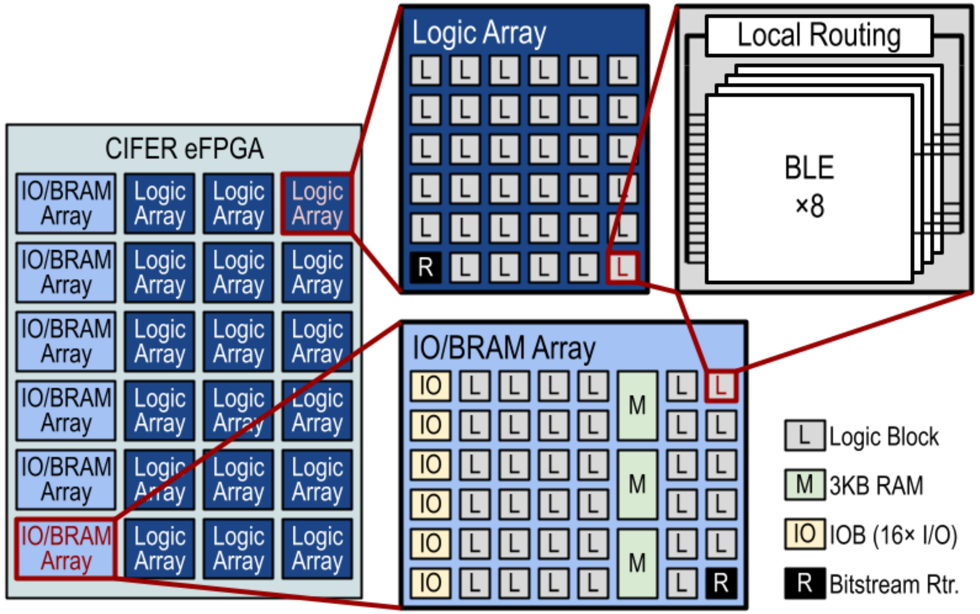
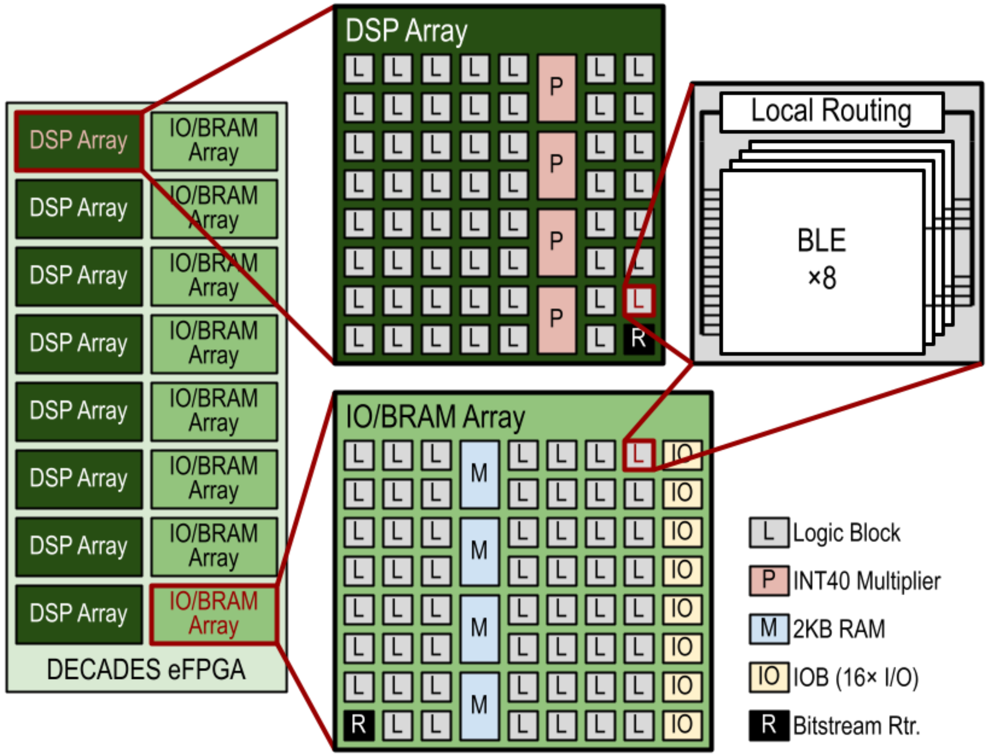


6 Unique Physical Blocks

DECADES eFPGA Hierarchy



7 Unique Physical Blocks

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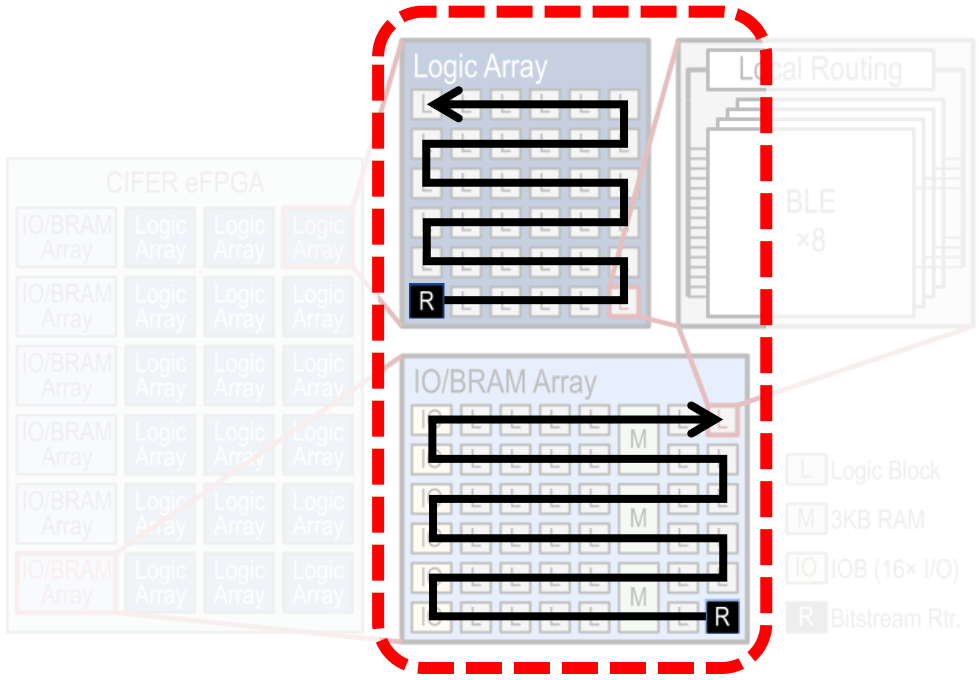
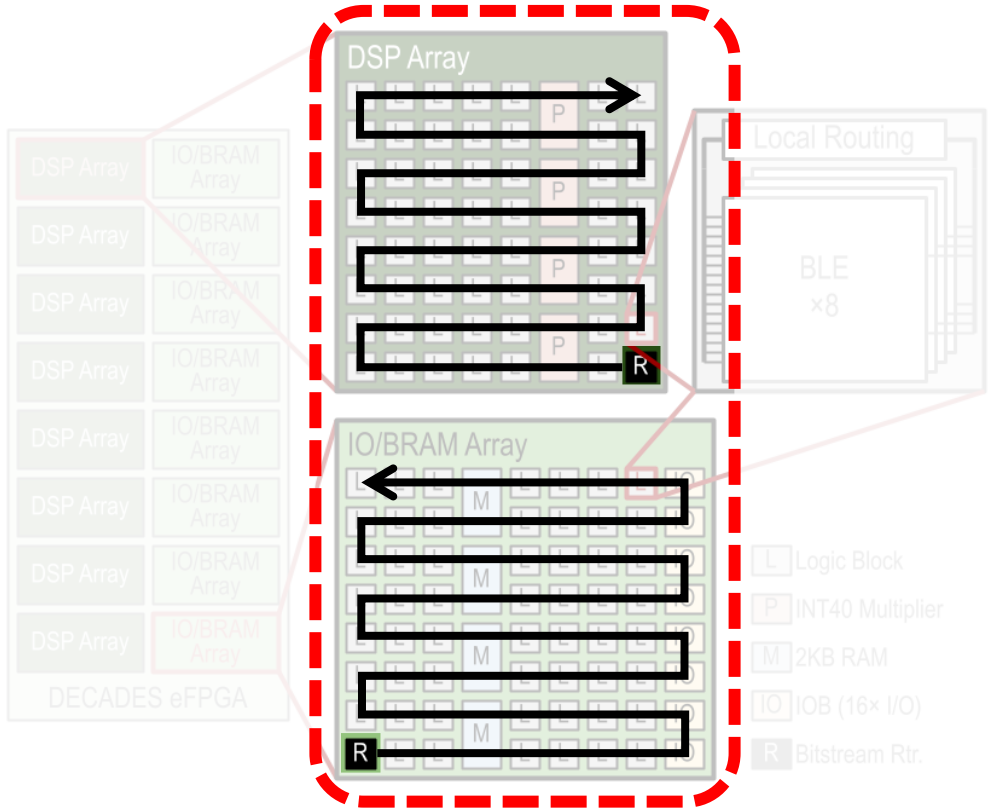
CIFER eFPGA



DECADES eFPGA



1-bit D-Flipflop Scan-chain within Sub-Arrays

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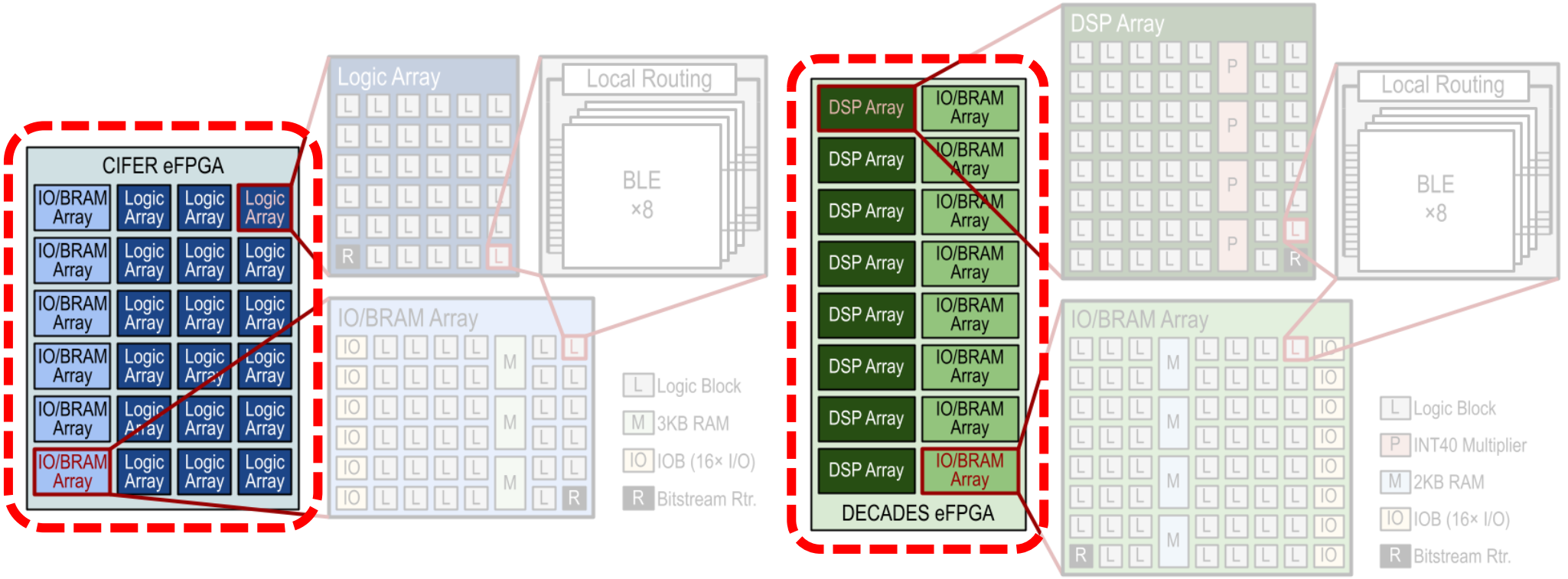
CIFER eFPGA

DECADES eFPGA



8-bit Packet-Switched Network between Sub-Arrays

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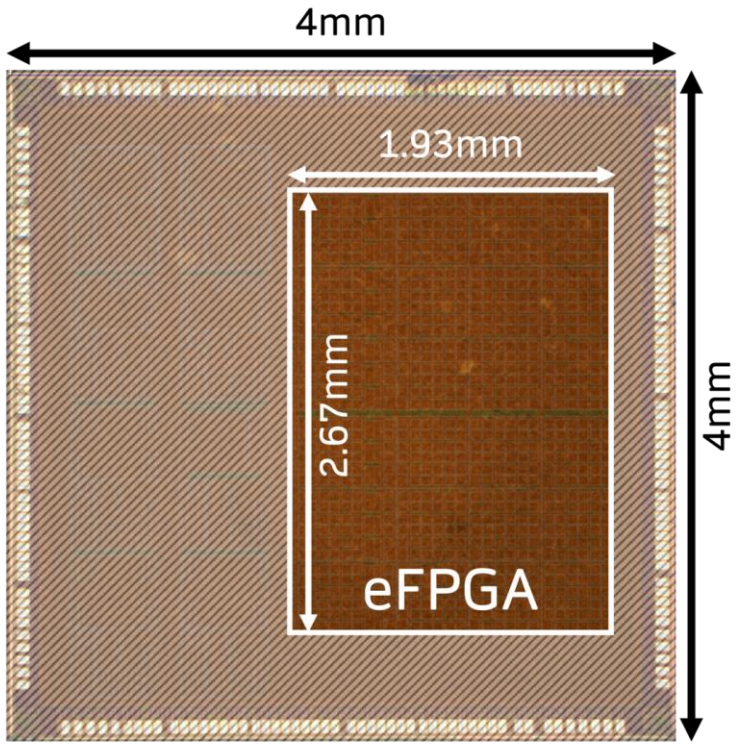
CIFER eFPGA



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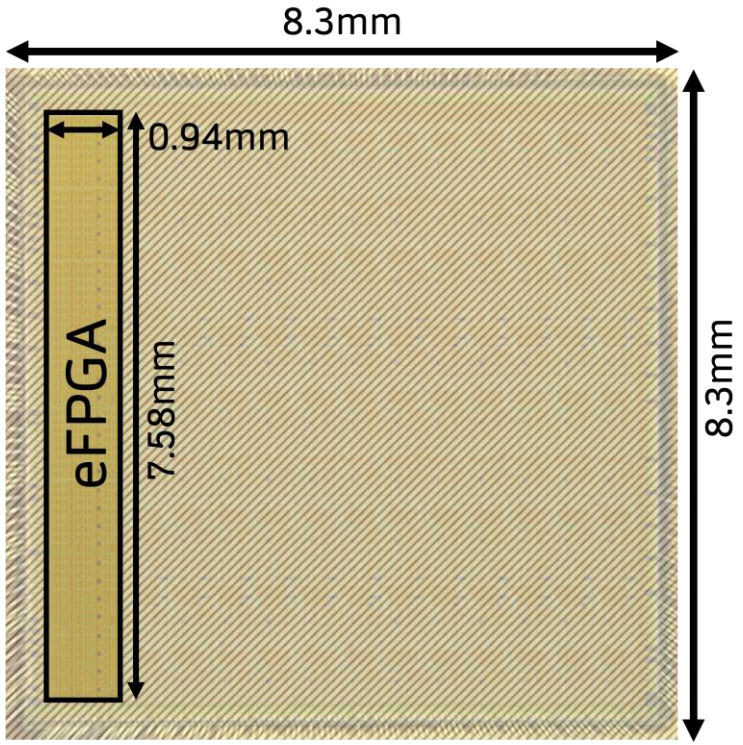

12nm FinFET | Standard Cells | SRAM Compiler

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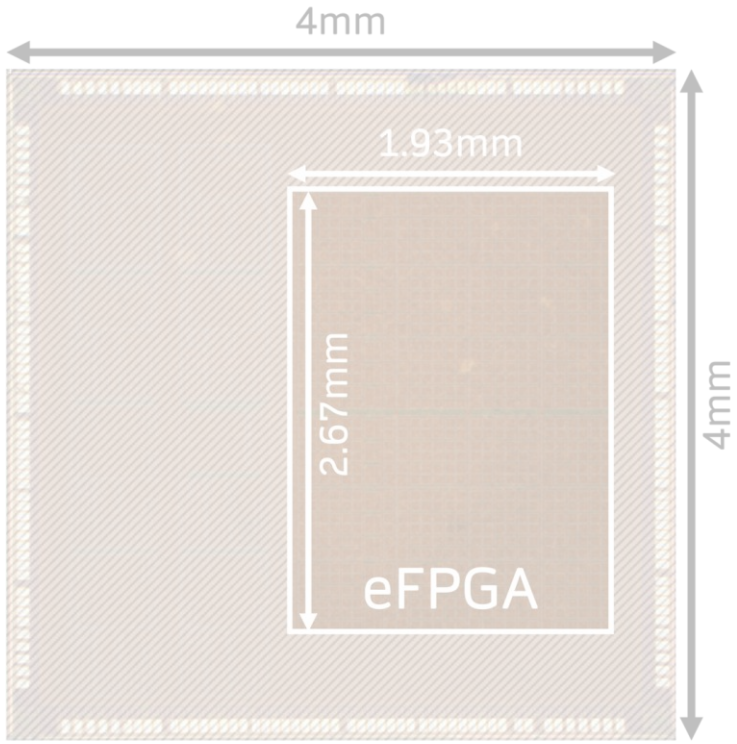
CIFER eFPGA



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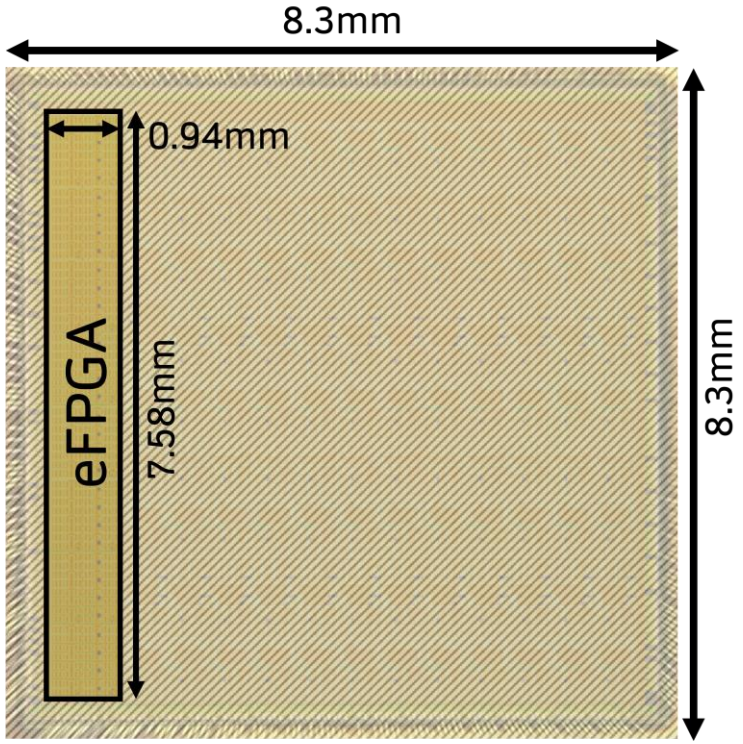

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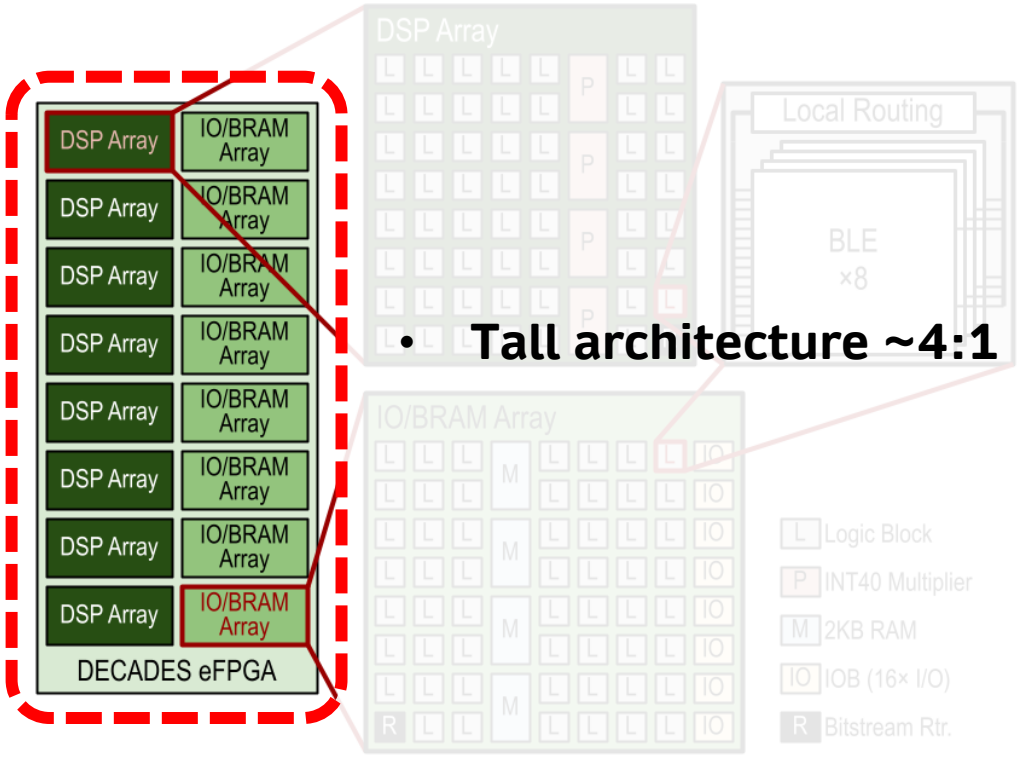
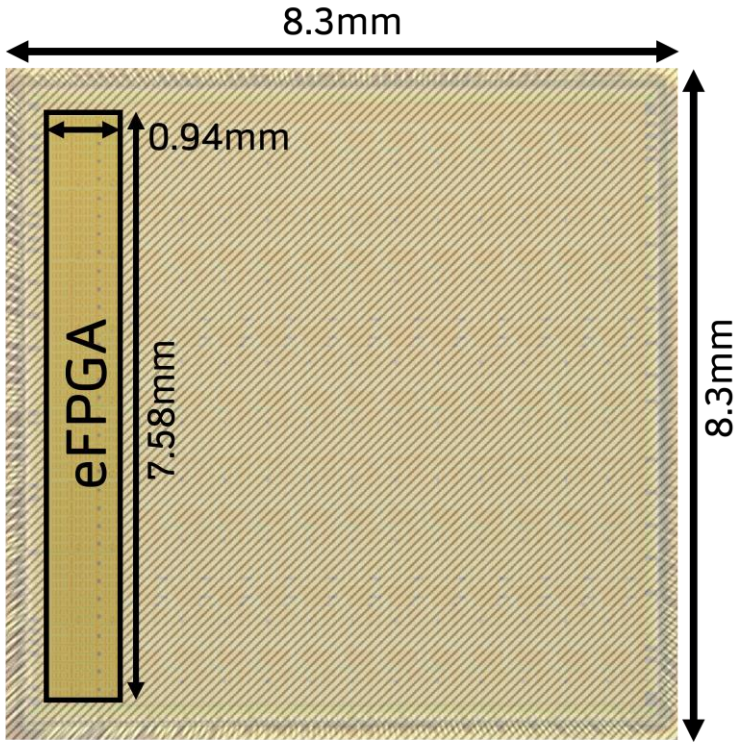


- **Tall architecture ~4:1**

DECADES eFPGA



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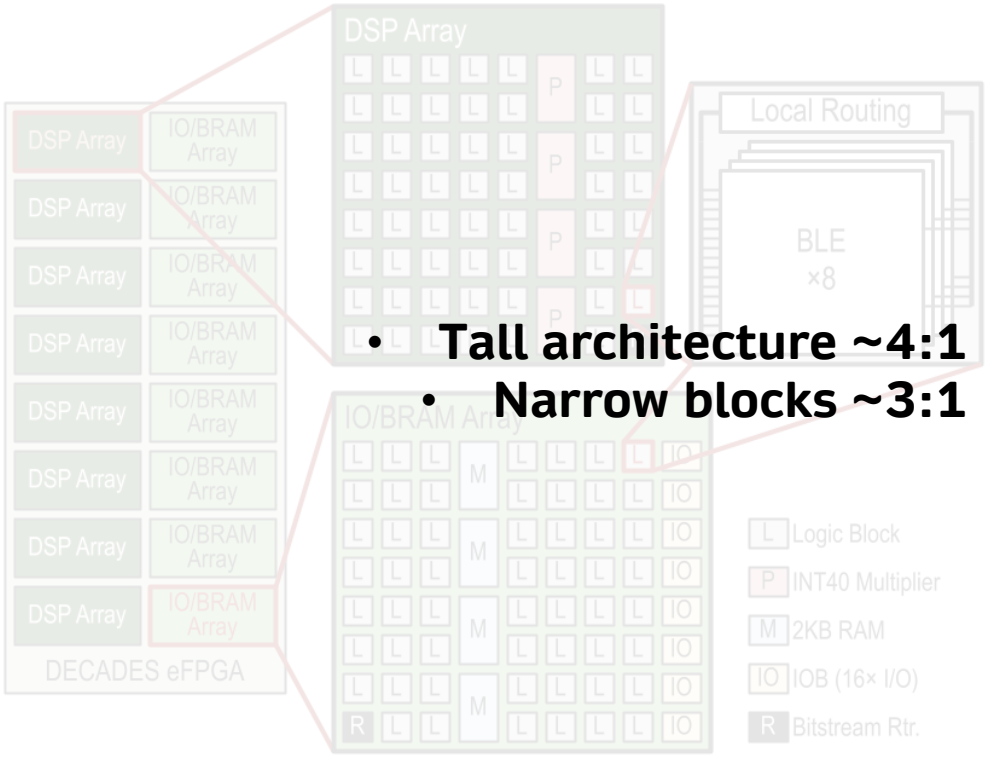
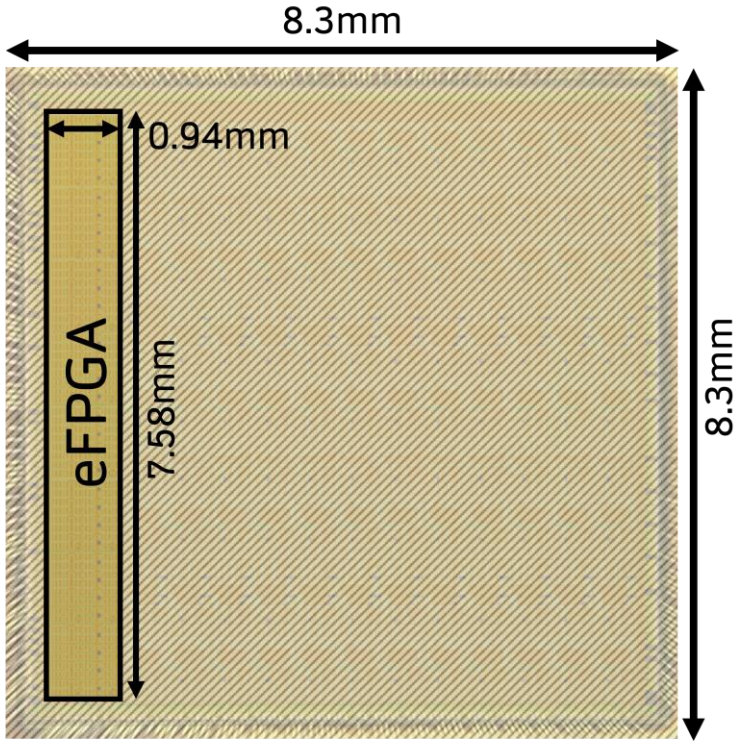


- **Tall architecture ~4:1**
- **Narrow blocks ~3:1**

DECADES eFPGA



:(Narrow Aspect Ratio >8:1

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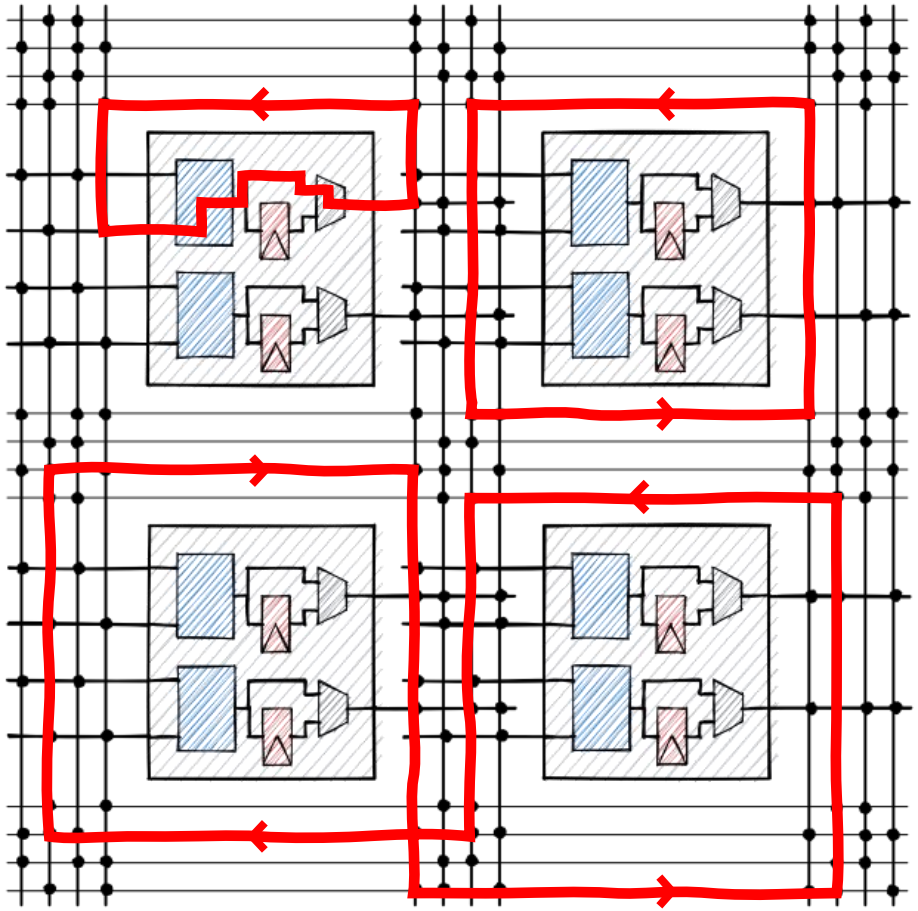
Timing Constraints

- Cycle-free FPGA[1]
  - Eliminates combinational loops in FPGA architectures



1. Ang Li, Ting-Jung Chang, and David Wentzlaff, "Automated Design of FPGAs Facilitated by Cycle-Free Routing", FPL'20

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Timing Constraints

- Cycle-free FPGA[1]
  - Eliminates combinational loops in FPGA architectures
- Config clock
  - **H-tree did not work**
    - Clock buffering -> huge area
    - Couldn't reach <1000 DRC
  - **Clock mesh**
    - >1GHz
    - Consumes a lot of power!

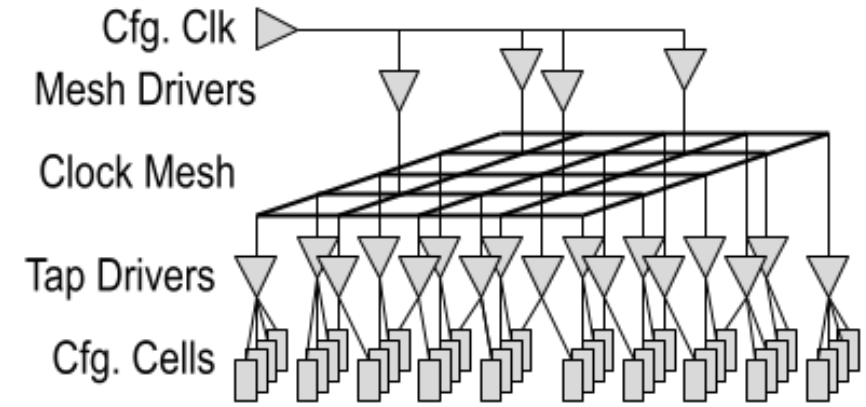

Illustration of the multi-source, cfg. clk mesh
(This clock structure is NOT a novelty of this work)

1. Ang Li, Ting-Jung Chang, and David Wentzlaff, "Automated Design of FPGAs Facilitated by Cycle-Free Routing", FPL'20

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SYN, PnR, STA, DRC, LVS, LEC, DFM …

- Same methodology as digital VLSI design using standard cell libraries

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Verification

- RTL testing with **no** problem
  - Emulation-over-simulation
- Gate-level simulation problems:
  - Zero-/Unit-delay gatesim: glitch amplification
    - Combinational loops through LUTs
  - SDF-annotated gatesim: couldn’t get it to work…

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- PRGA
- CIFER eFPGA & DECADES eFPGA
  - Architecture
  - Physical Design
- Evaluation
- Conclusion

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CIFER eFPGA vs. Commercial eFPGA

	Logic Resources			Performance			Efficiency
	LUT6	BRAM (Kbit)	Logic Density (LUT6/mm^2)	Fmax† (MHz)	INT8‡ GOPS	INT8‡ MOPS/LUT	INT8‡ GOPS/W
Baseline*	8760	0	1991	747	56.5	6.45	312.4
CIFER	6720	432	1541	300	12.9	1.92	148.1
%	**76.71%**	-	**77.40%**	**40.16%**	**22.83%**	**29.77%**	**47.41%**

* Baseline: flexlogix AI + eFPGA commercial **eFPGA** in TSMC **16nm** [1]

† Fmax benchmark: [*baseline*] INT16 FFT-32; [*CIFER*] 64-bit LFSR

‡ Performance/Efficiency benchmark: [*baseline*] GEMM; [*CIFER*] INT8-complex FFT-64

1. S. K. Lee, P. N. Whatmough, M. Donato, G. G. Ko, D. Brooks and G. -Y. Wei, *"SMIV: A 16-nm 25-mm^2 SoC for IoT With Arm Cortex-A53, eFPGA, and Coherent Accelerators,"* JSSC'22

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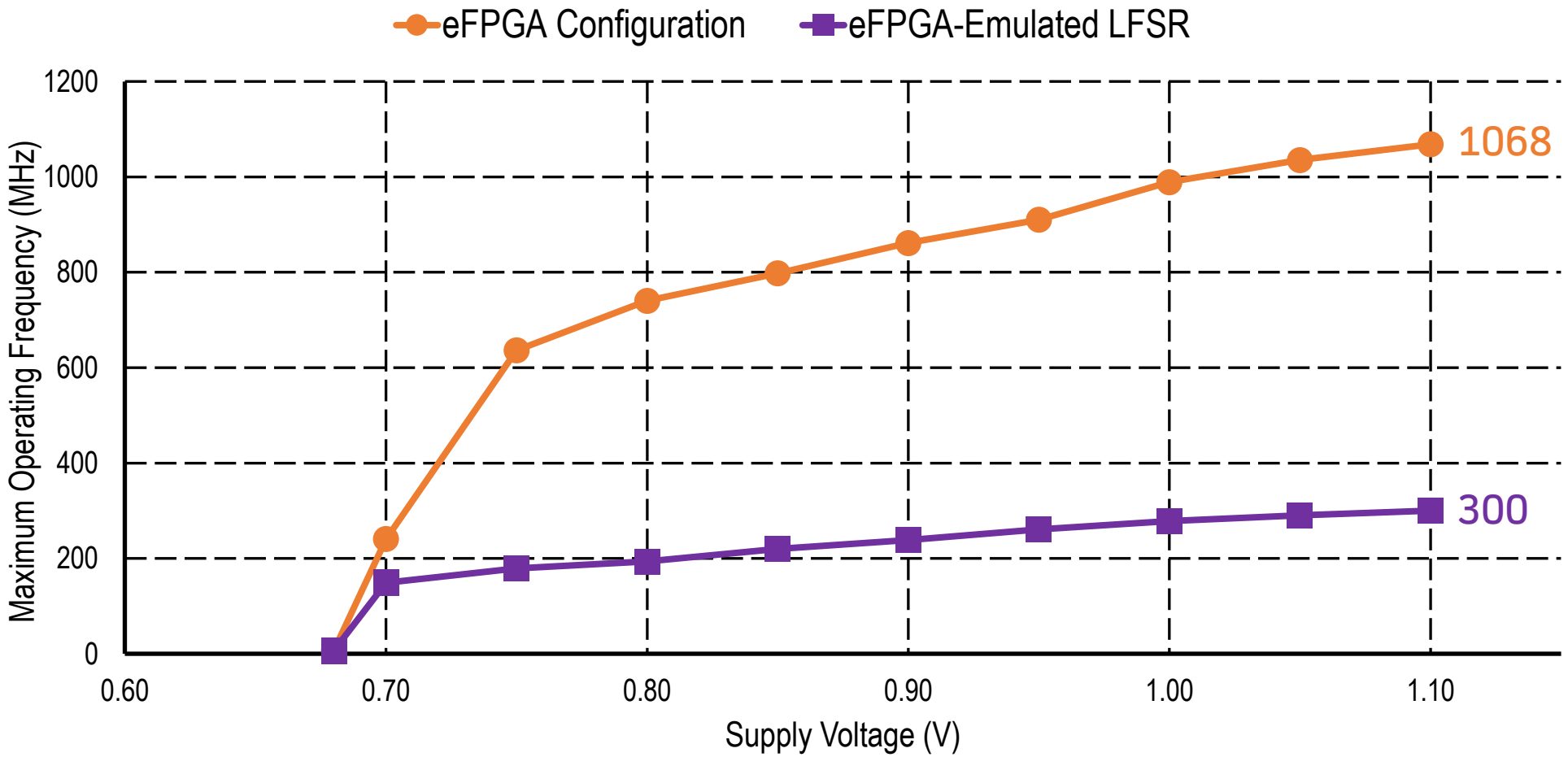
CIFER eFPGA F_{max}



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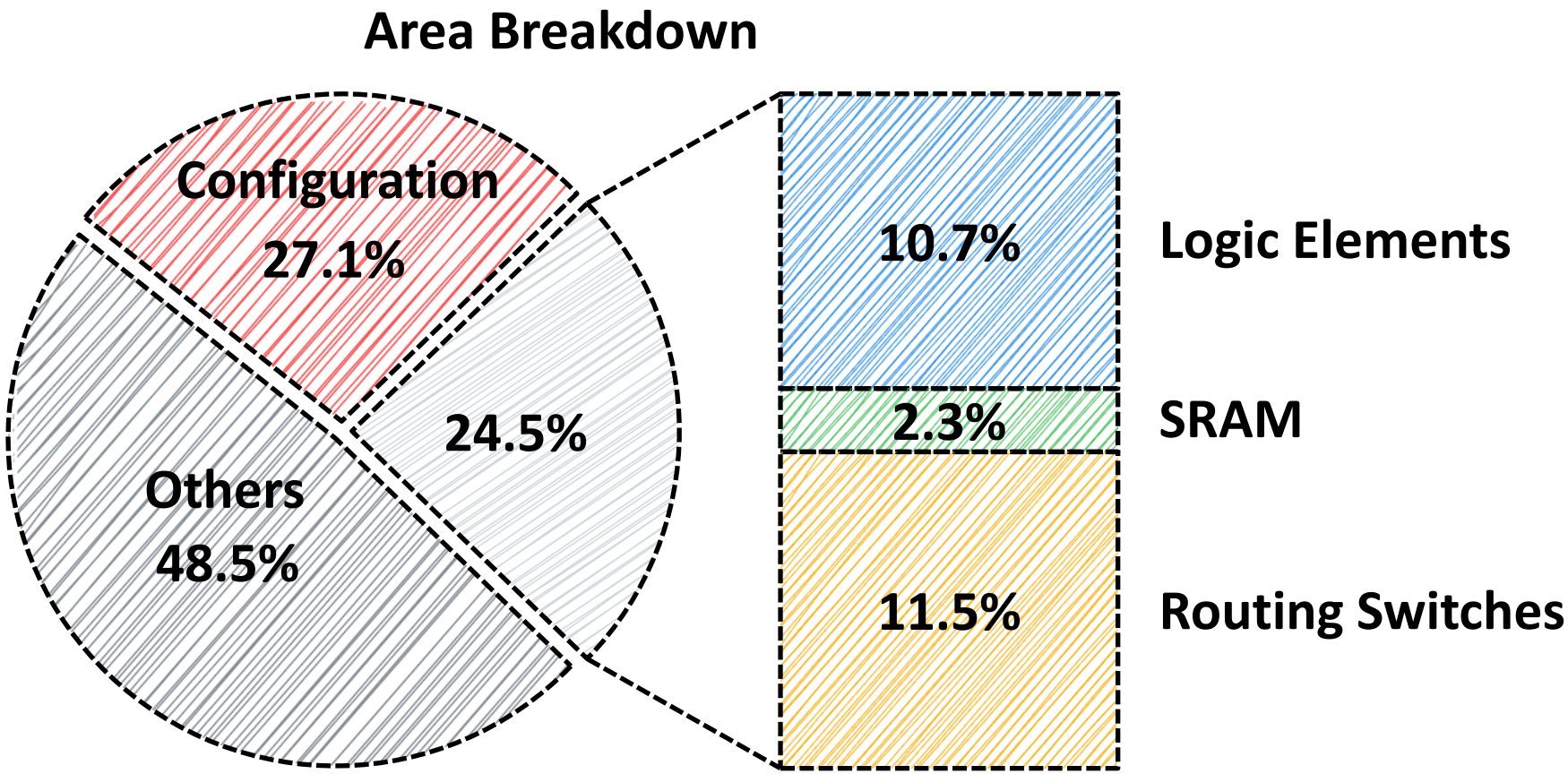
CIFER eFPGA Area Breakdown



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DECADES eFPGA vs. CIFER eFPGA

	LUT			Multiplier			Efficiency (GOPS/W)	
	Used	Avail.	Util.	Used	Avail.	Util.		
CIFER	6041	6720	**89.9%**	0	0	0.0%	148.1	
DECADES	2276	7040	**32.3%**	24	32	**75.0%**	170.6	**(+15.2%)**

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Conclusion

- PRGA: silicon-proven, open-source FPGA IP
- CIFER eFPGA & DECADES eFPGA

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Conclusion

- PRGA: silicon-proven, open-source FPGA IP
- CIFER eFPGA & DECADES eFPGA
- :(Notable gaps to commercial standards
- :) Lots of low-hanging optimizations available

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Thank You!