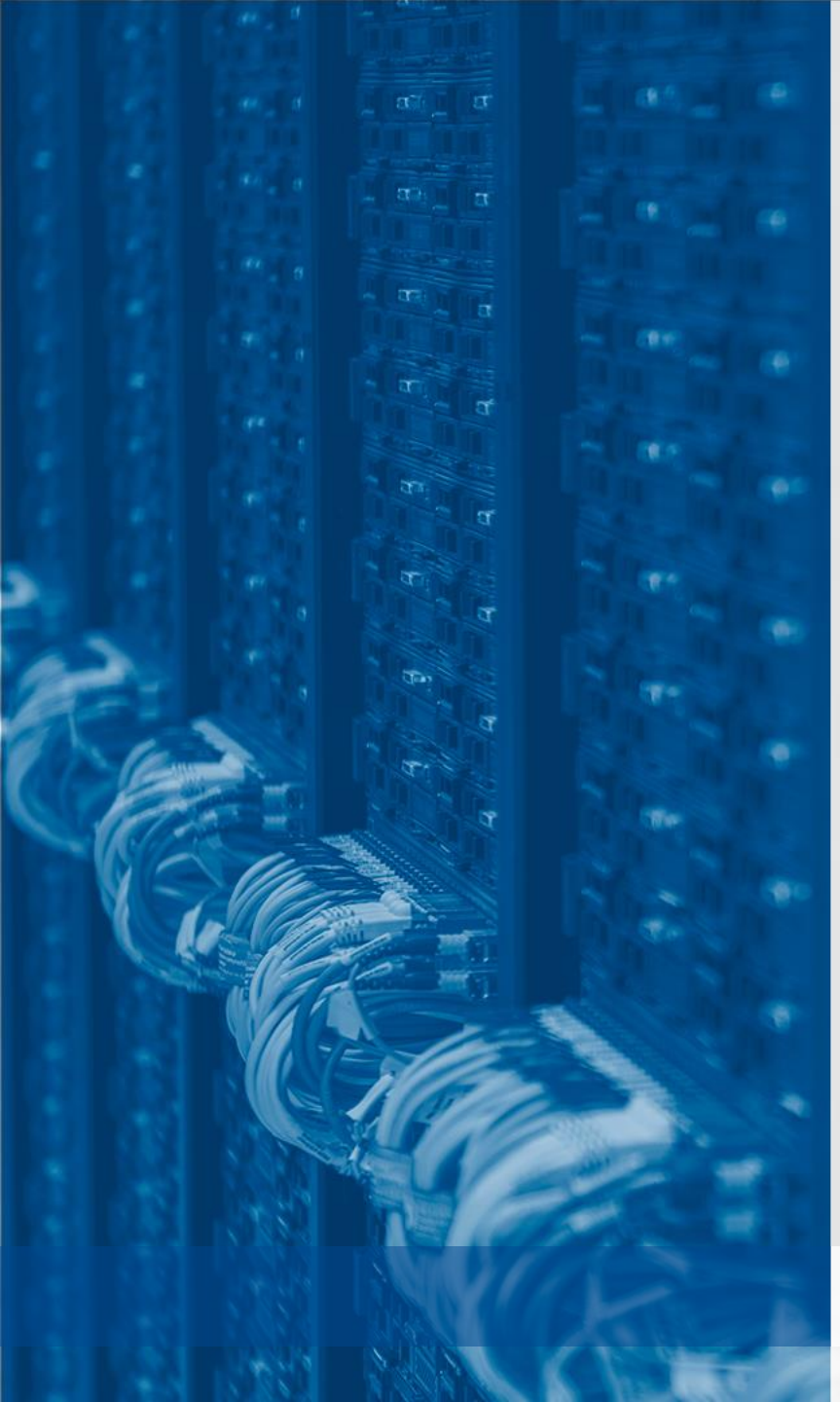

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

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UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

Past, Present and Future of Designing, Integrating and Simulating RTL Models

Guillem López Paradís, Jonathan Balkind,
Adrià Armejach, Miquel Moretó

OSCAR 2024

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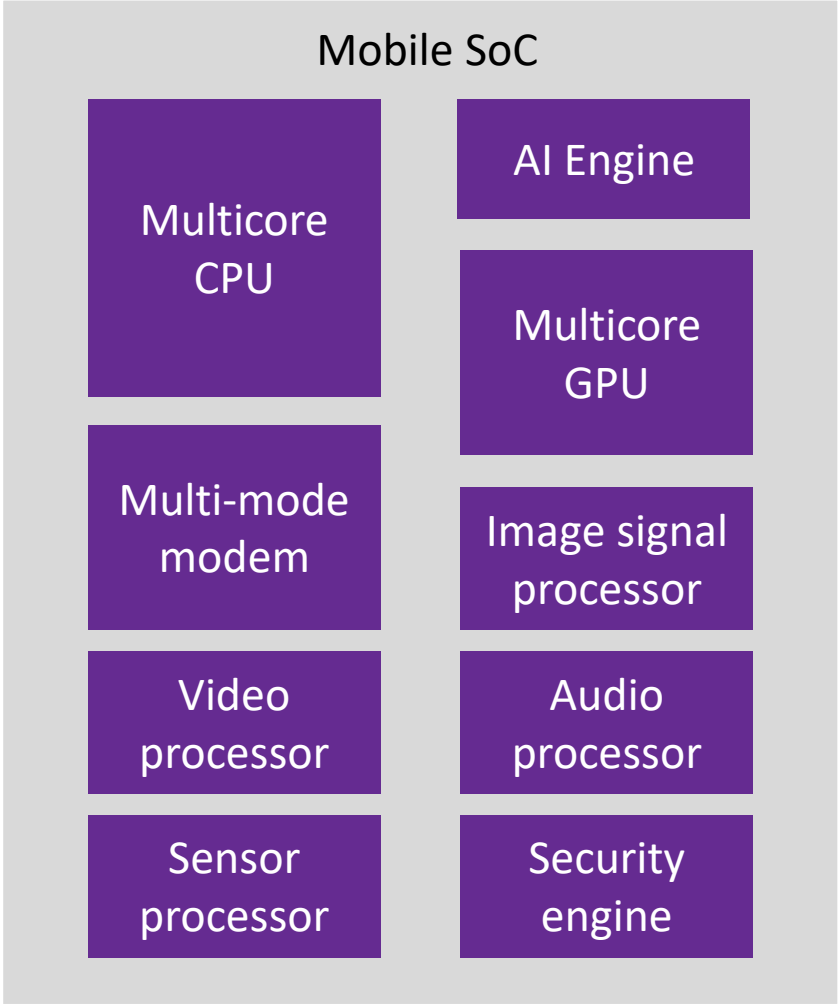

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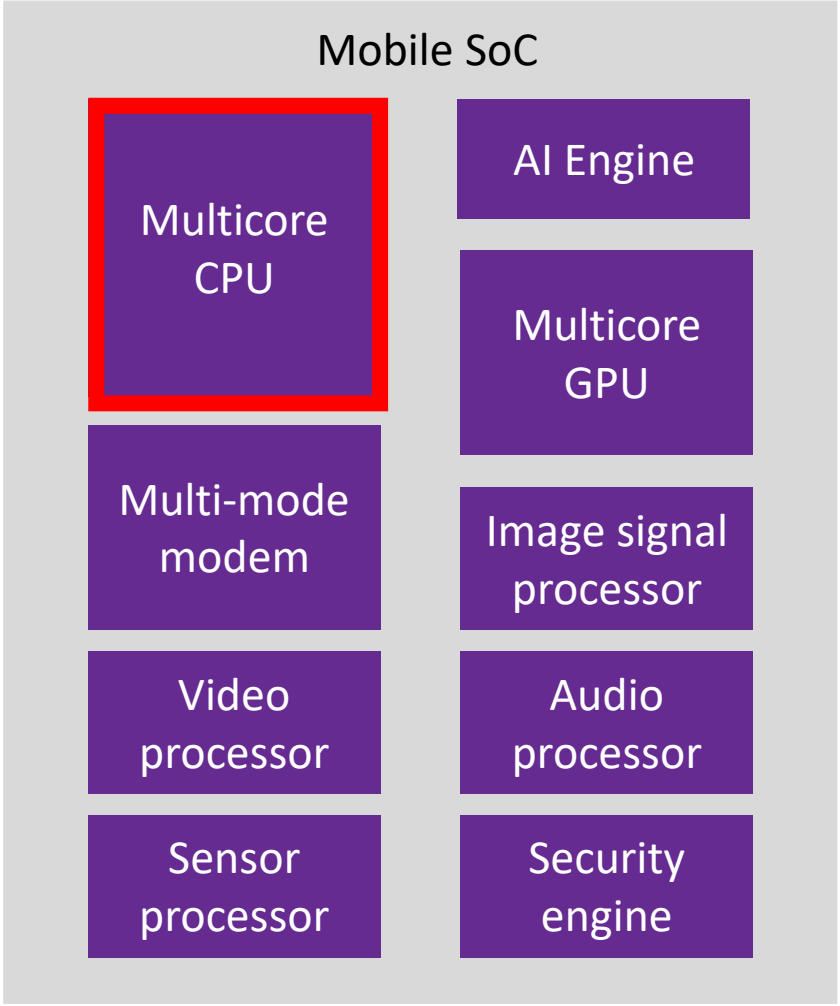

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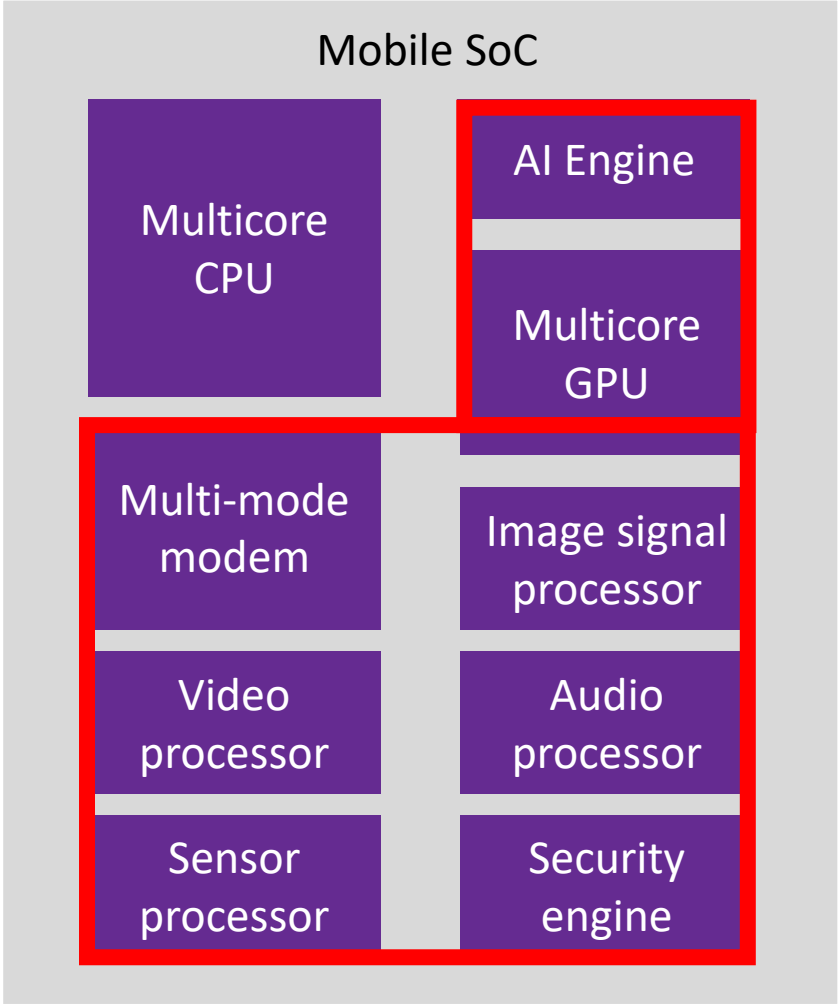

Motivation

- Boom in fabricating new hw
- Heterogeneous hardware on the same SoC requires complex integration and verification processes
- **Improve the tools to verify large-scale hardware designs!**

Outline

- **Gem5+RTL: A Full-System RTL Simulation Infrastructure**

- Fast Behavioural RTL Simulation of 10B Transistor SoC Designs with Metro-MPI

Gem5+RTL Objectives

- Framework that **enables easy integration of existing RTL hardware** blocks within a **SoC** for full-system simulations

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Gem5+RTL Objectives

- Framework that enables easy integration of existing RTL hardware blocks within a SoC for full-system simulations

- Deliver a comprehensive hardware/software ecosystem where all the main components of the SoC are present with a complete software stack

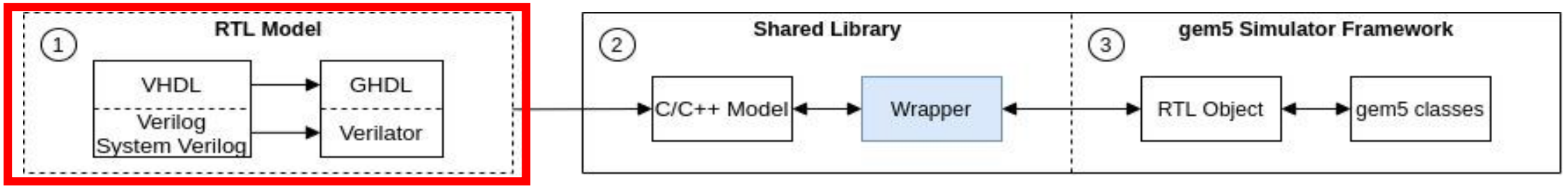
- **Enable testing** the **implemented functionality** of these hardware blocks and also, the **expected performance** they will provide on an existing **SoC design**

Framework Design

1. **We use Verilator and GHDL to obtain a C++ model from an RTL model written in Verilog/SystemVerilog and VHDL**

2. We provide a wrapper to interact with it and gem5. Then, the wrapper and the C++ model are combined into a shared library

3. In gem5, a generic framework is provided to ease the integration of a wide range of potential hardware designs: generic RTLObject class



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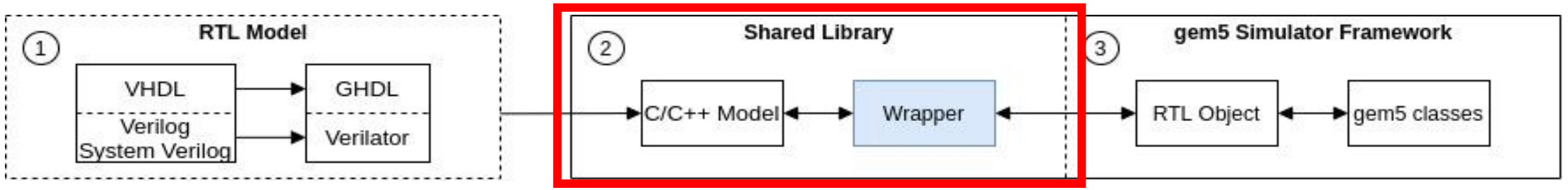

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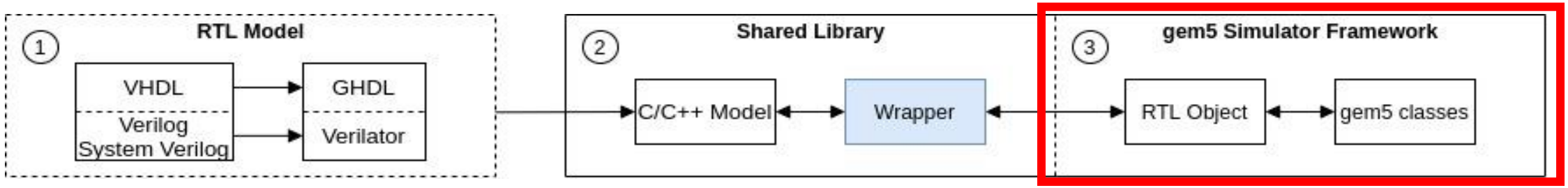
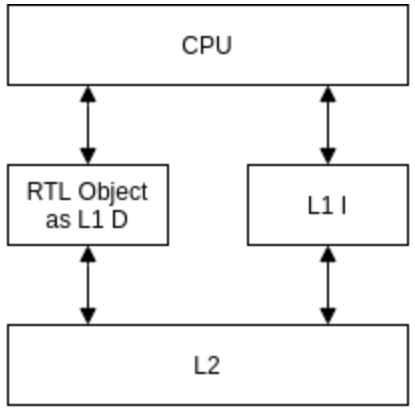


Connectivity Examples



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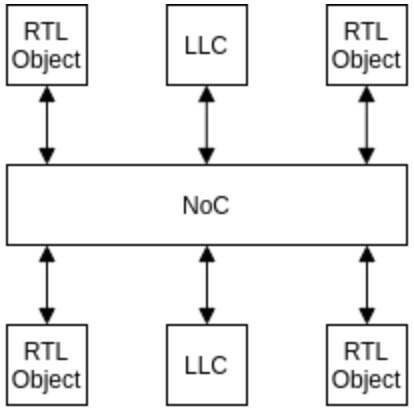

(b) NoC design exploration

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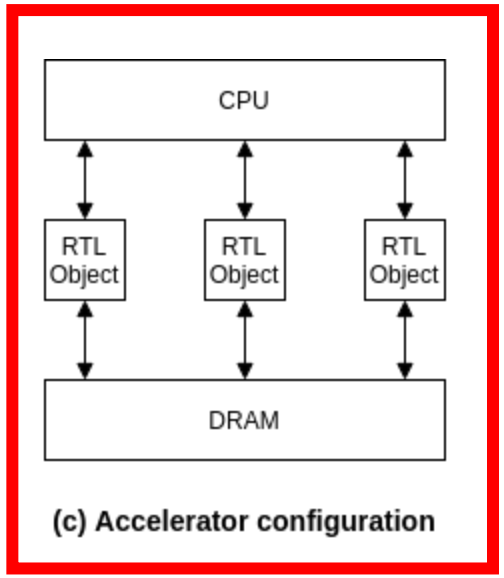

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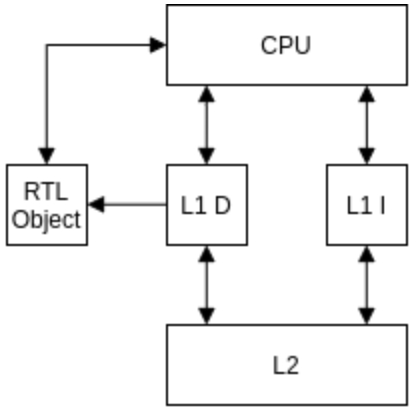

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Accelerator Use Case

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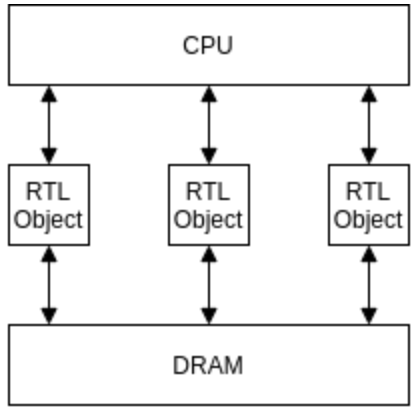

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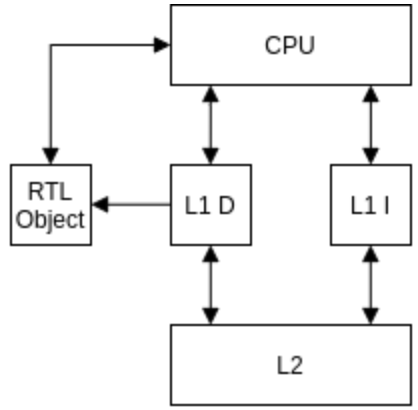

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Gem5+RTL

https://gitlab.bsc.es/glopez/gem5-rtl

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Motivation: RTL Simulation Performance

- **SoCs today are reaching 10B+ transistors in scale**

Name	#Cores	#Billions Transistors
Apple M2	8-12	20 - 67
AWS Graviton 3	64	55
Esperanto ET-SoC-1	1024	24

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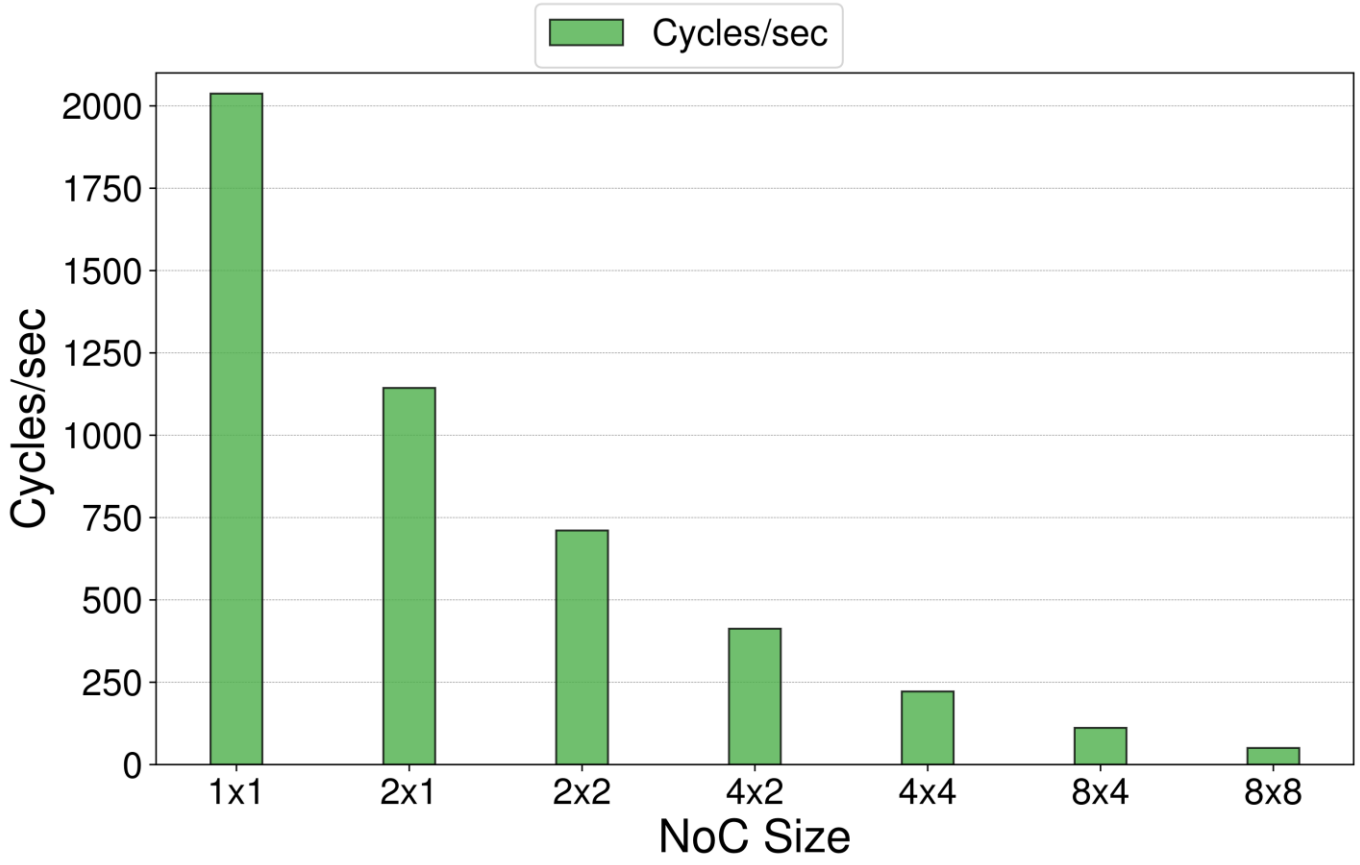

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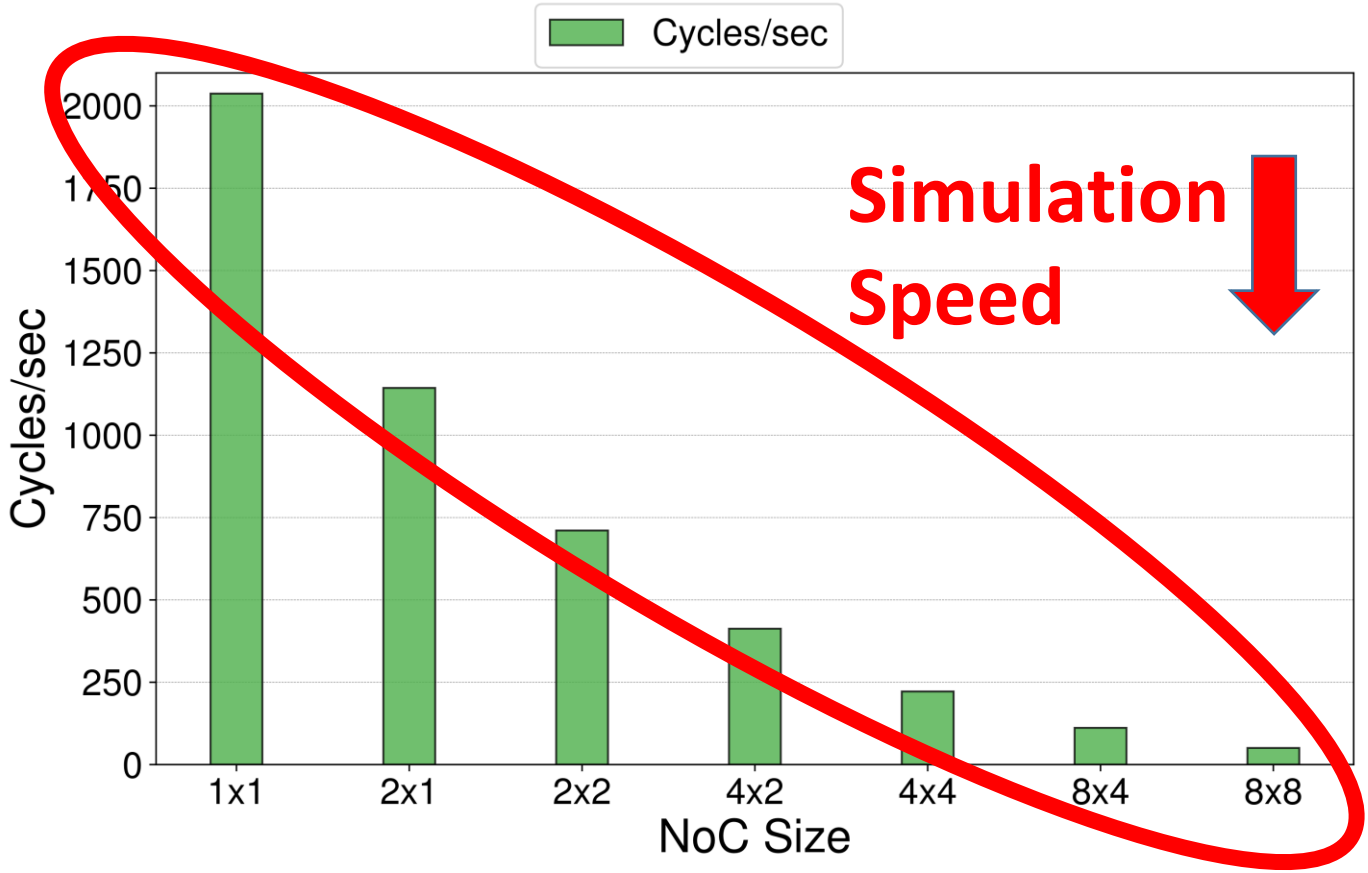
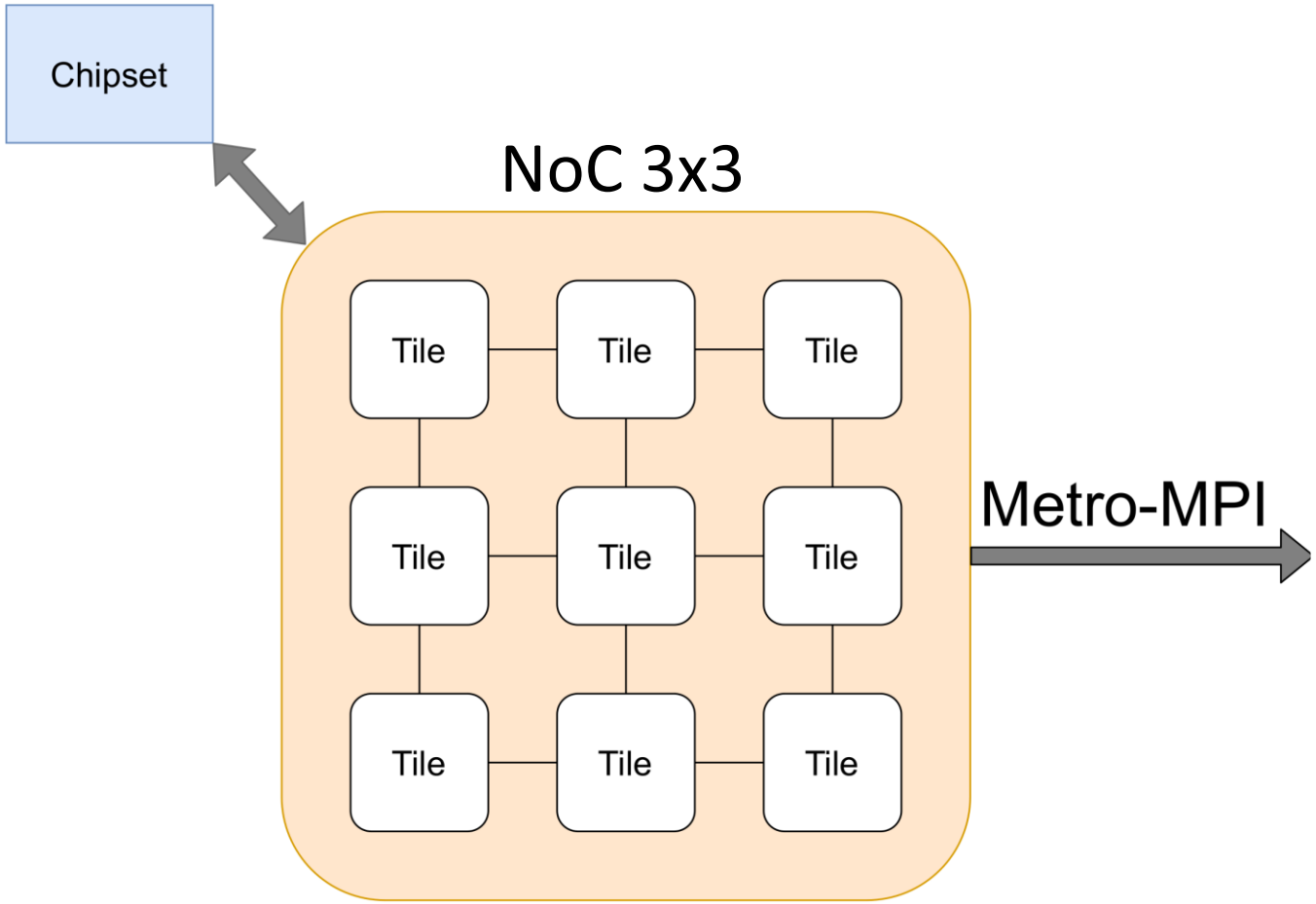


NoC RTL-Simulation with MPI



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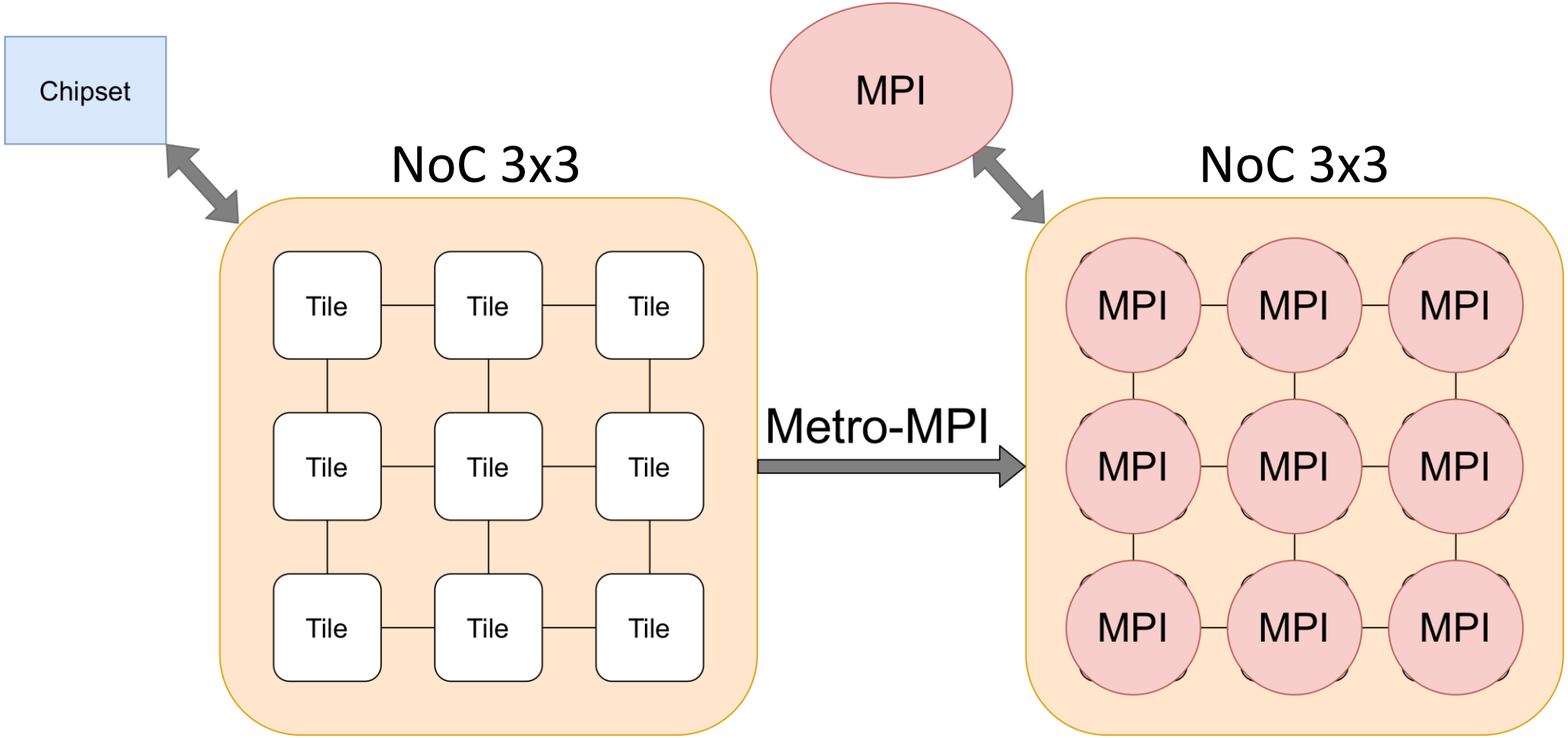

Exploting SoCs' Natural Boundaries

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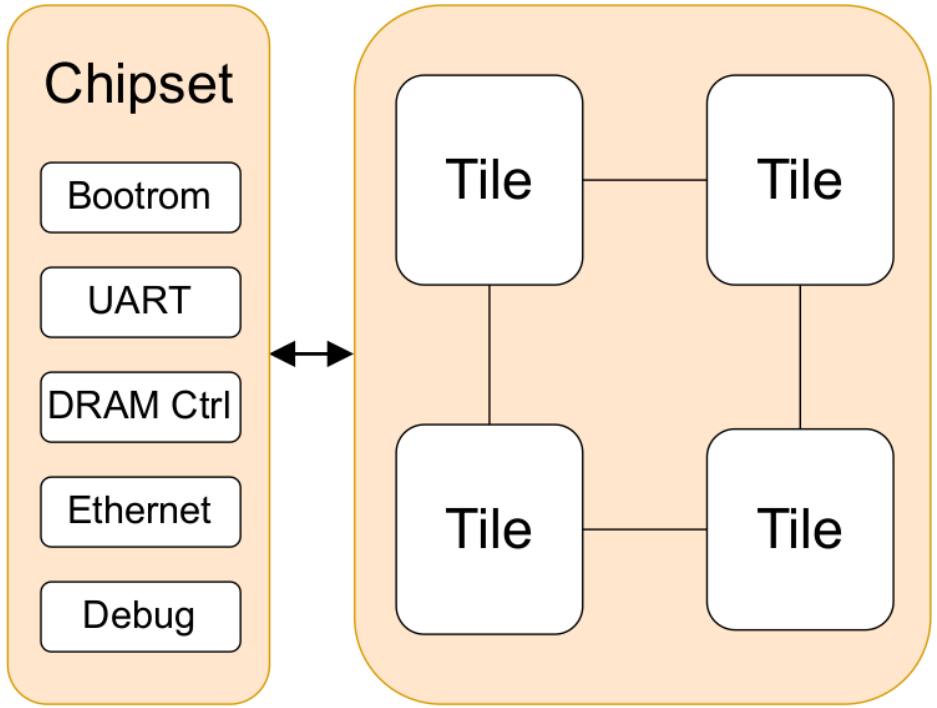

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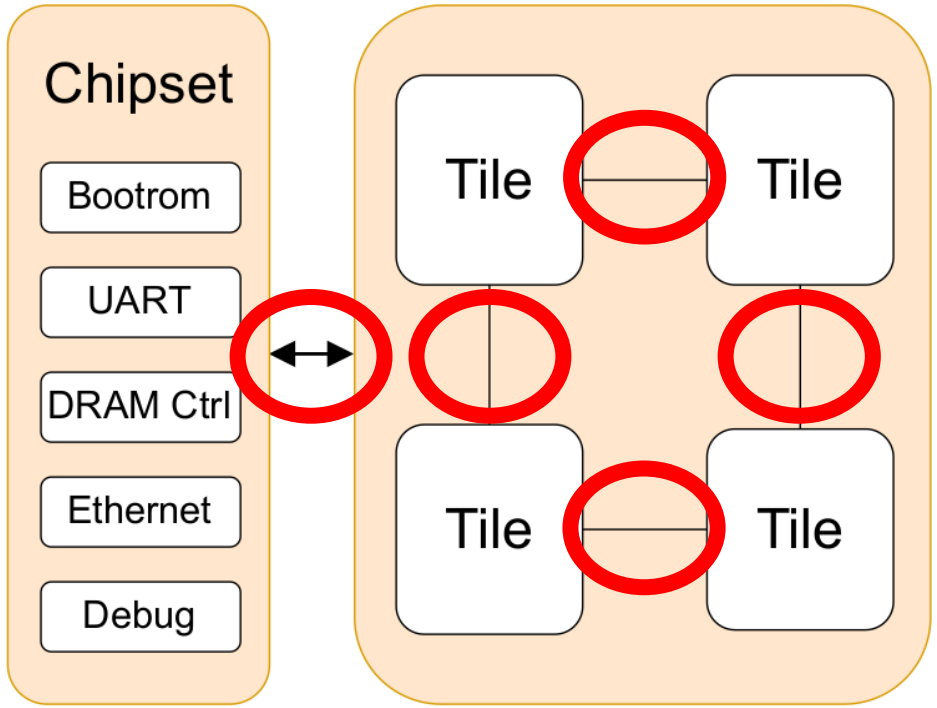

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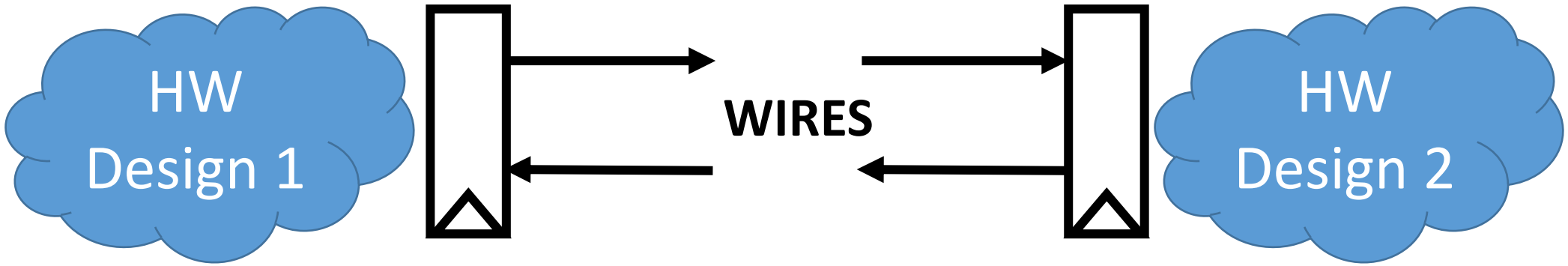

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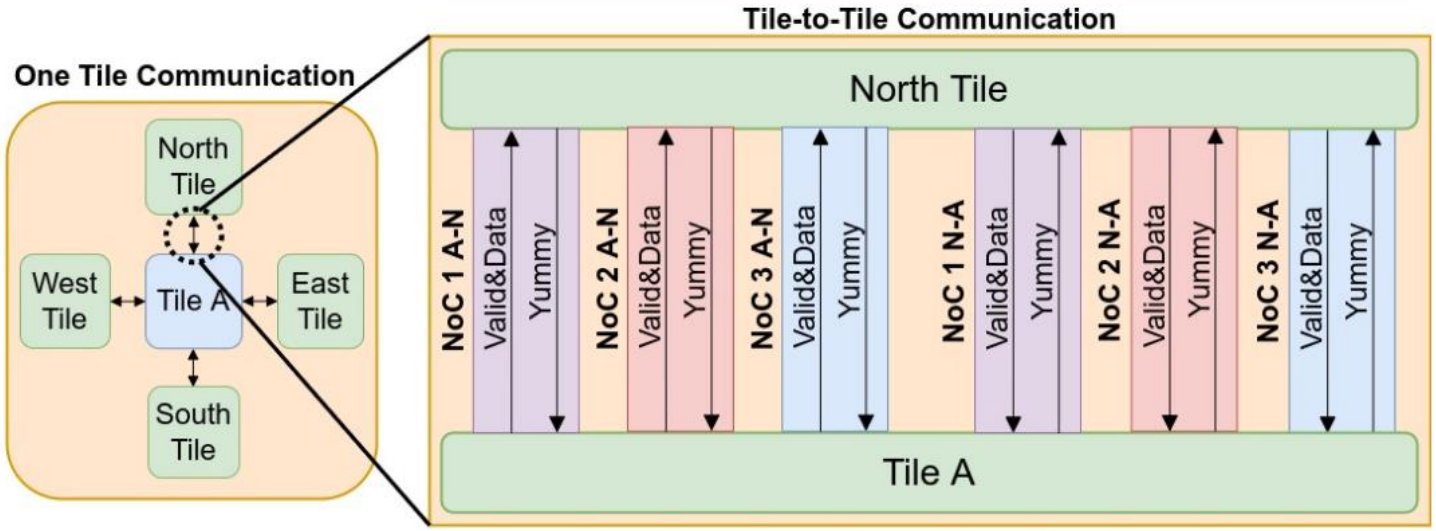

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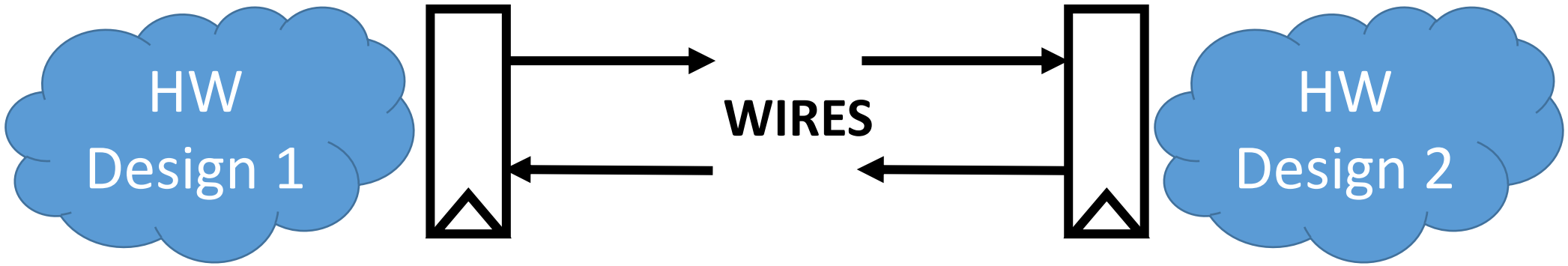

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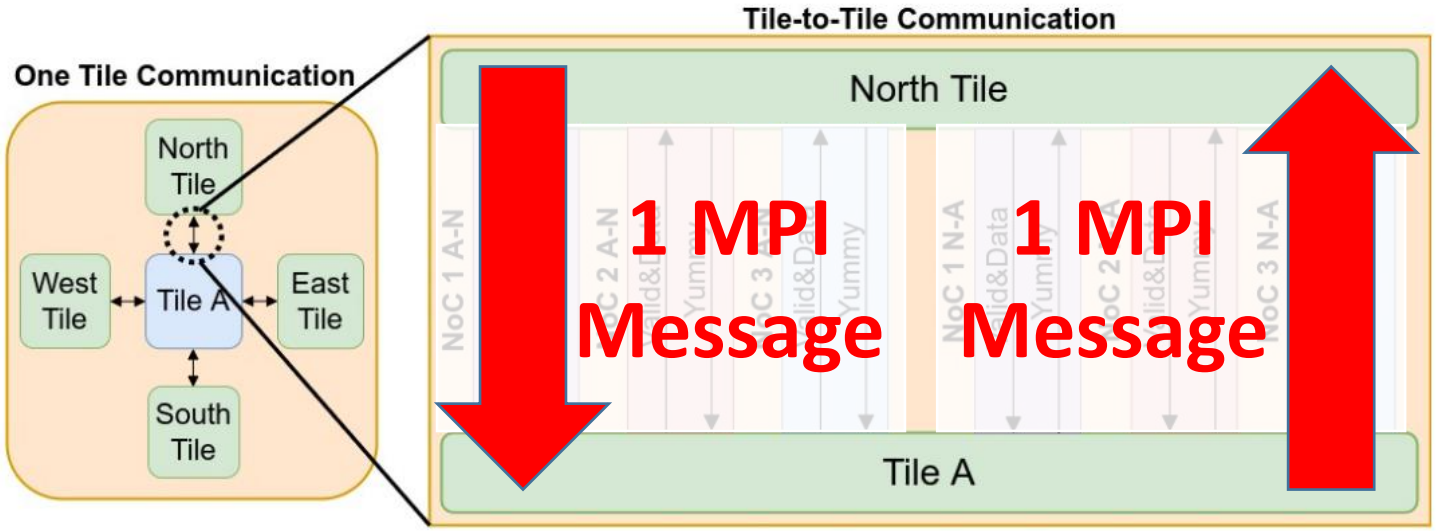

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Methodology

- **We use OpenPiton+Ariane → chip sizes from 1x1 to 32x32 (1024 tiles)**

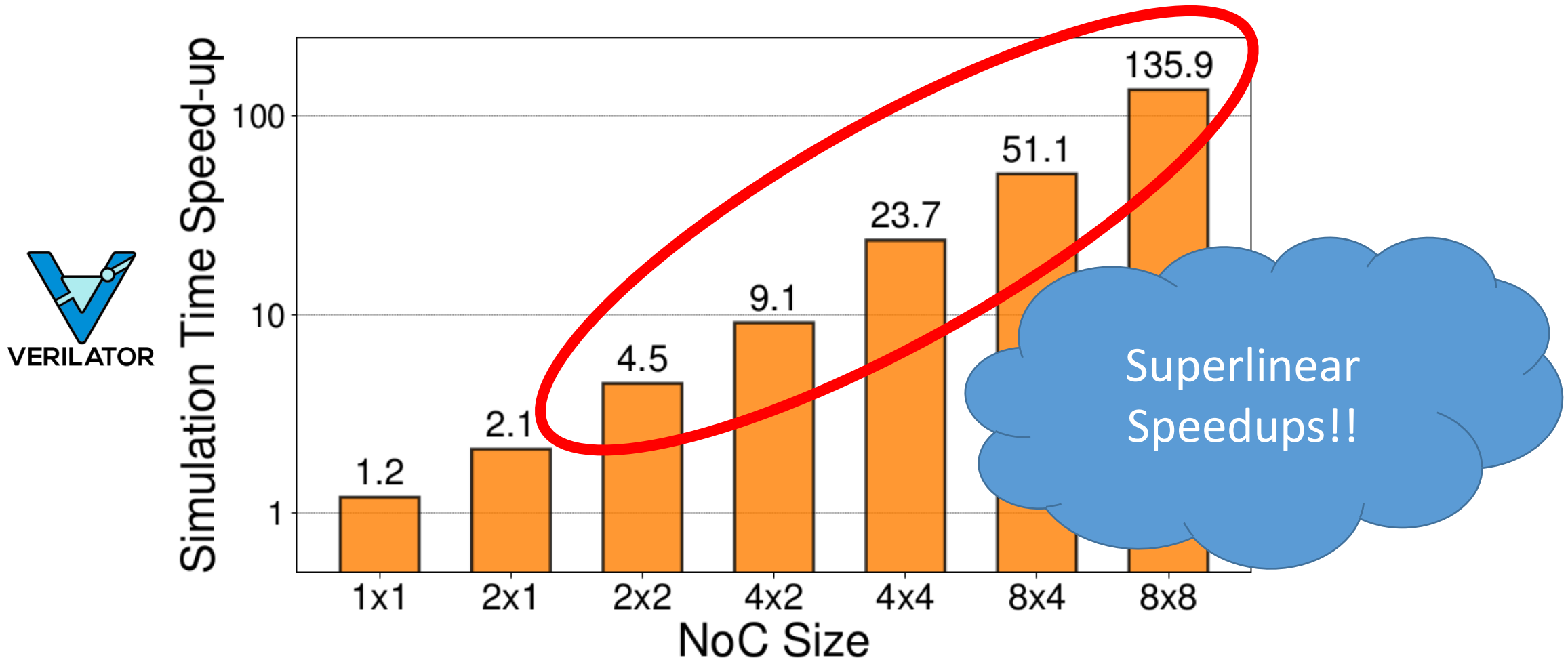
- **Testbench: Atomic synchronized token passing app**

Methodology

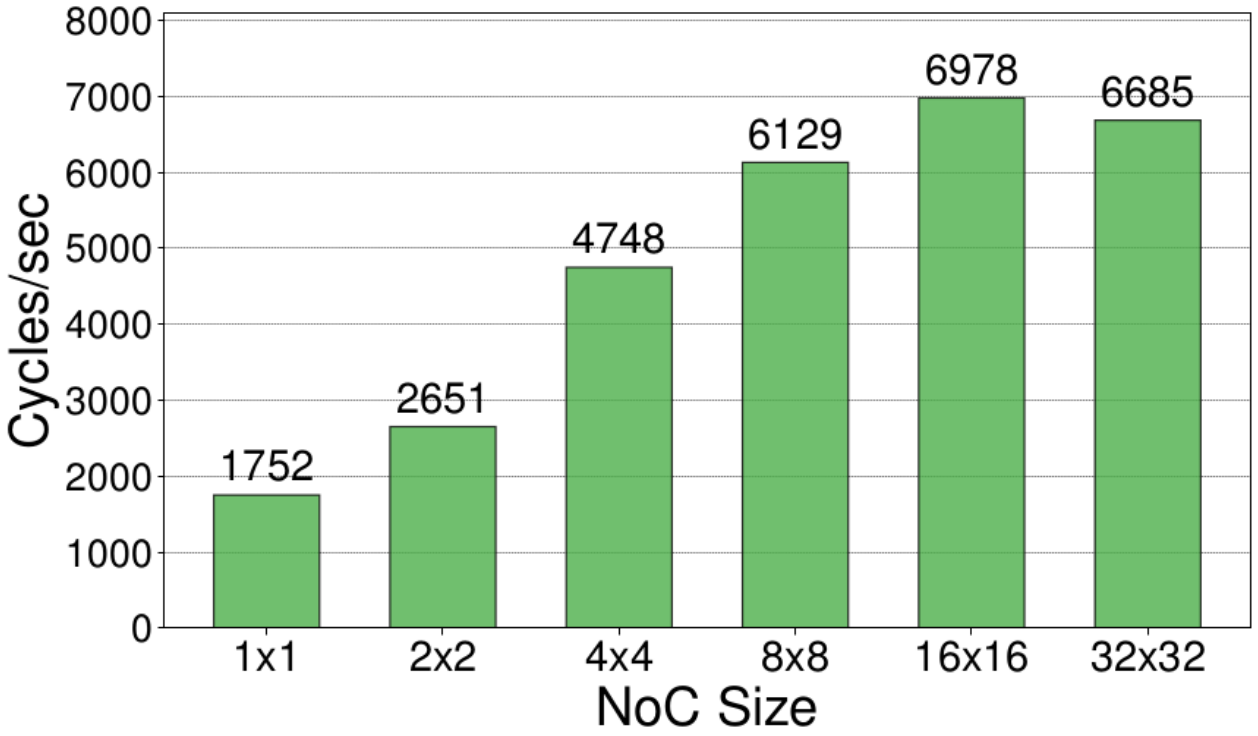
- We use OpenPiton+Ariane → chip sizes from 1x1 to 32x32 (1024 tiles)
- Testbench: Atomic synchronized token passing app
- **Simulators: Verilator and a "*Big 3*" RTL Simulator**
- **We use MareNostrum 4 Supercomputer with 100Gbs Network**
  - **1 Node has 48 cores**

NoC Size	1x1	4x4	32x32
#MPI/Cores	2	17	1025
#Nodes	1	1	22

Metro-MPI Simulation Time Speedup



Metro-MPI Simulated Cycles/sec



VERILATOR

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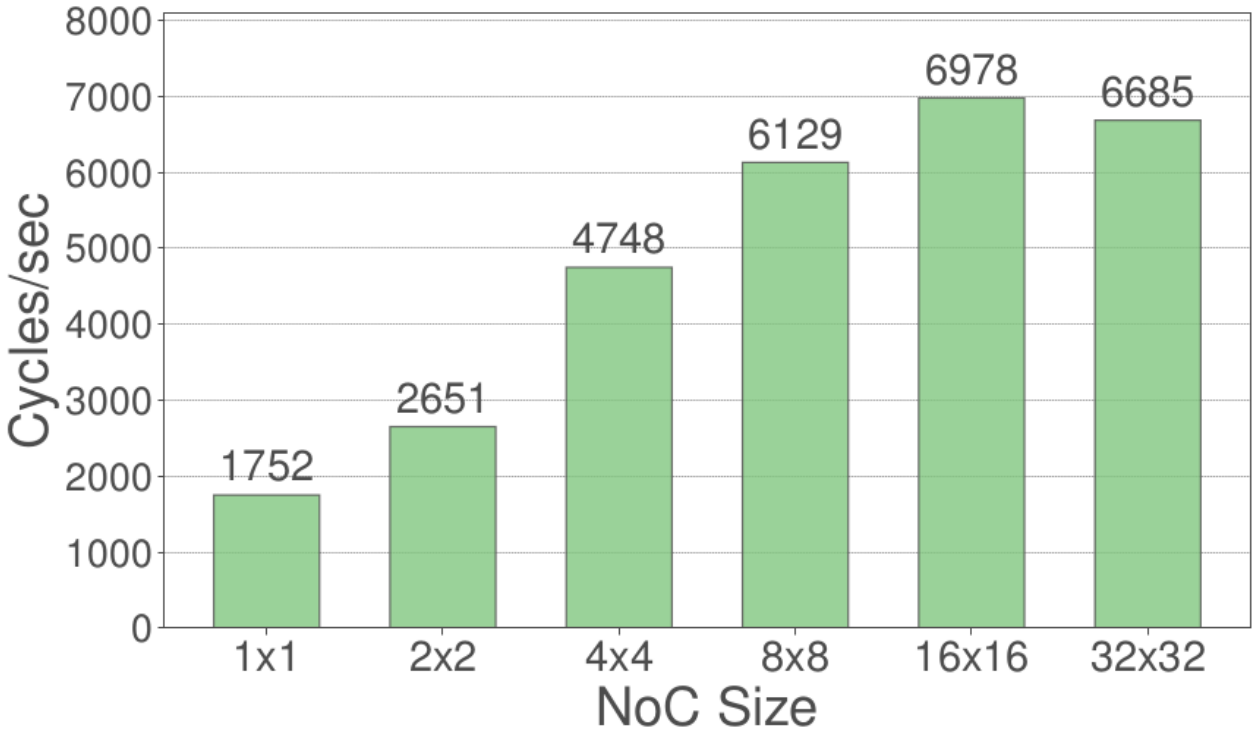

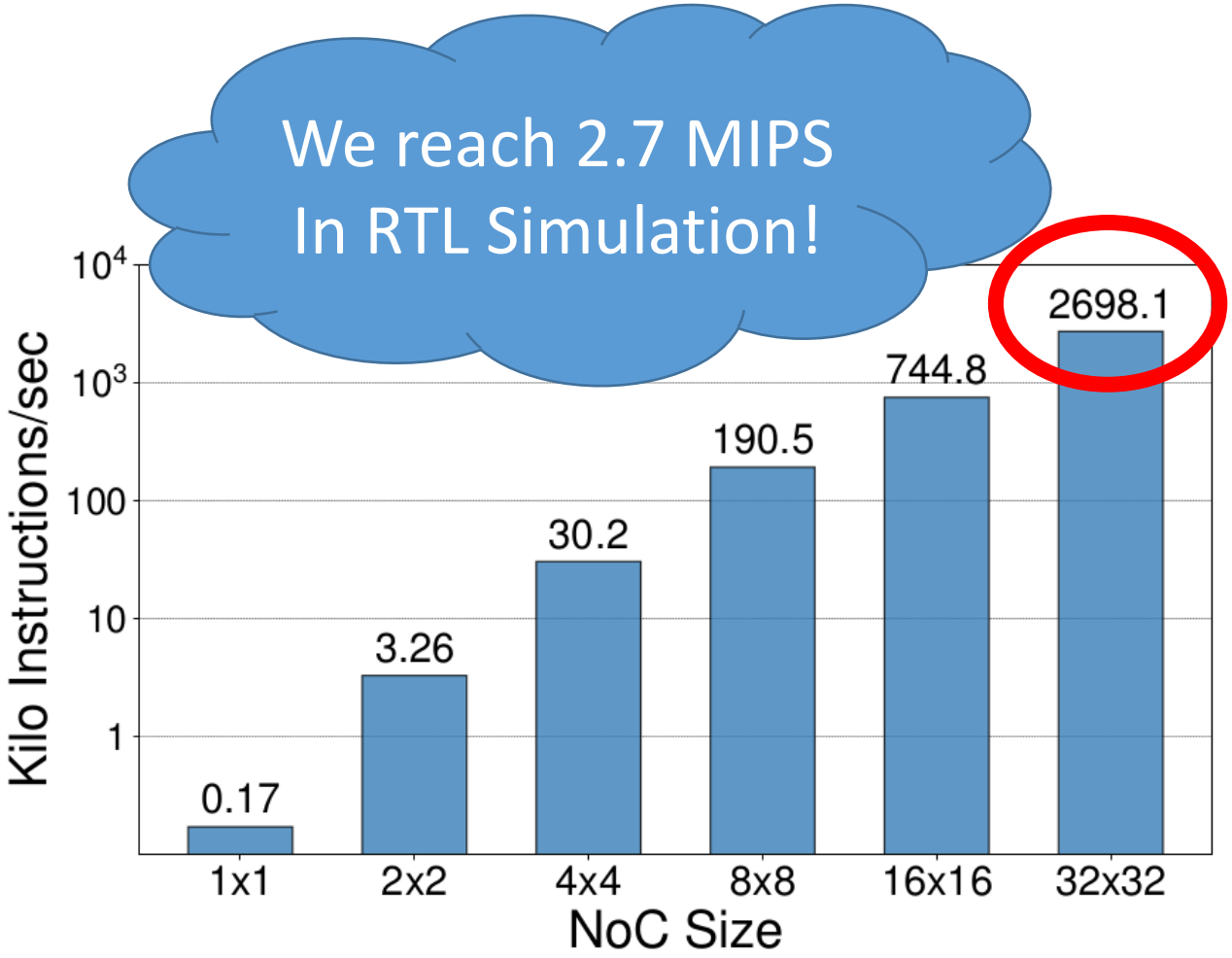

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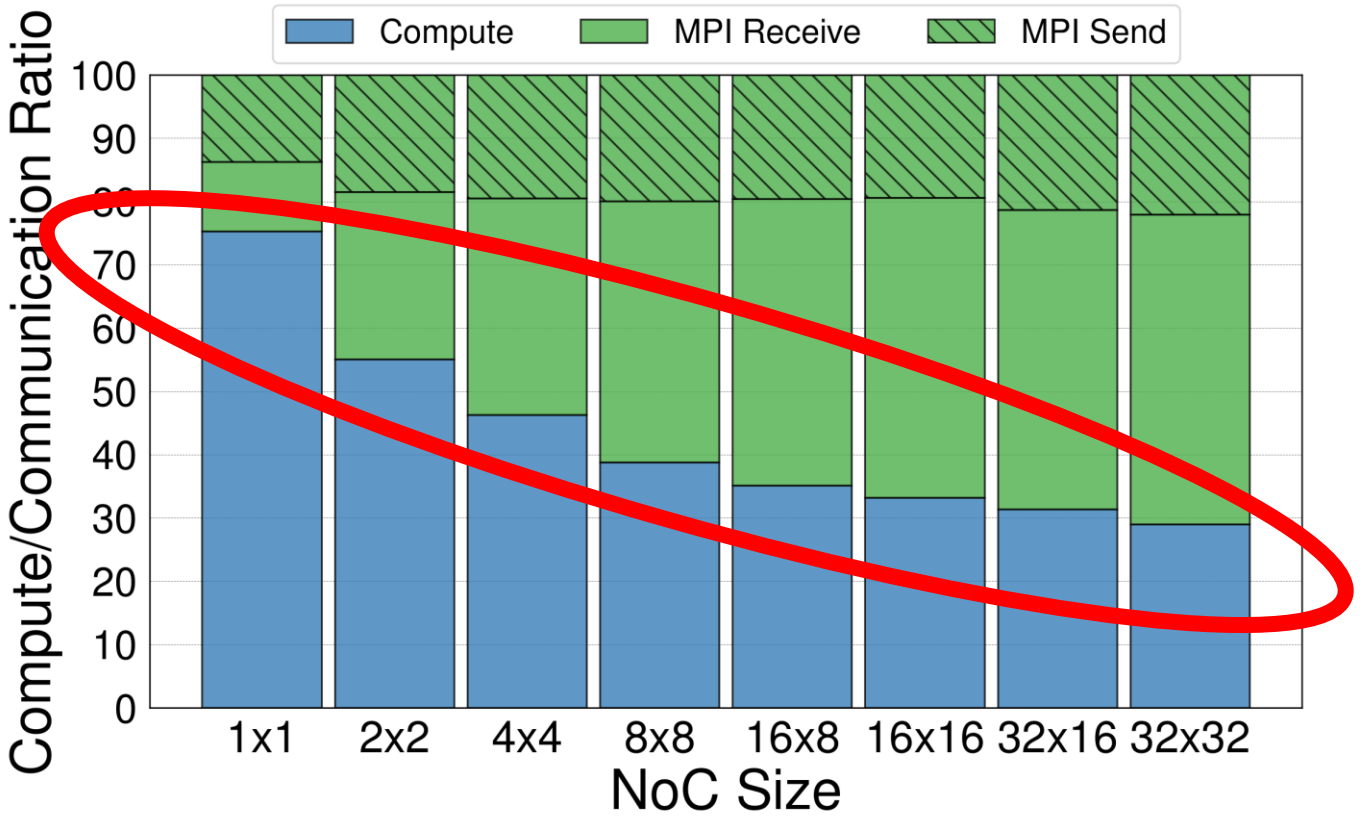

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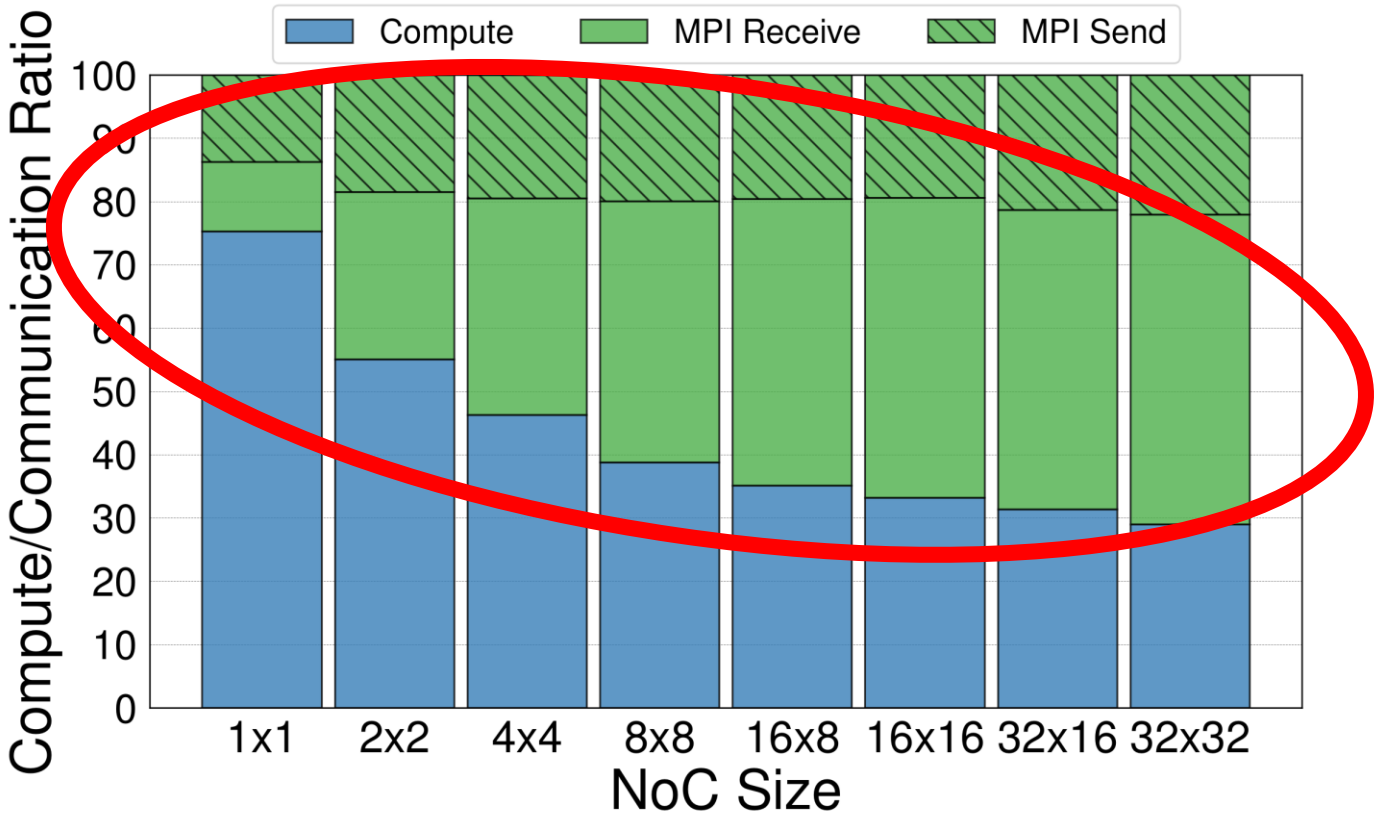

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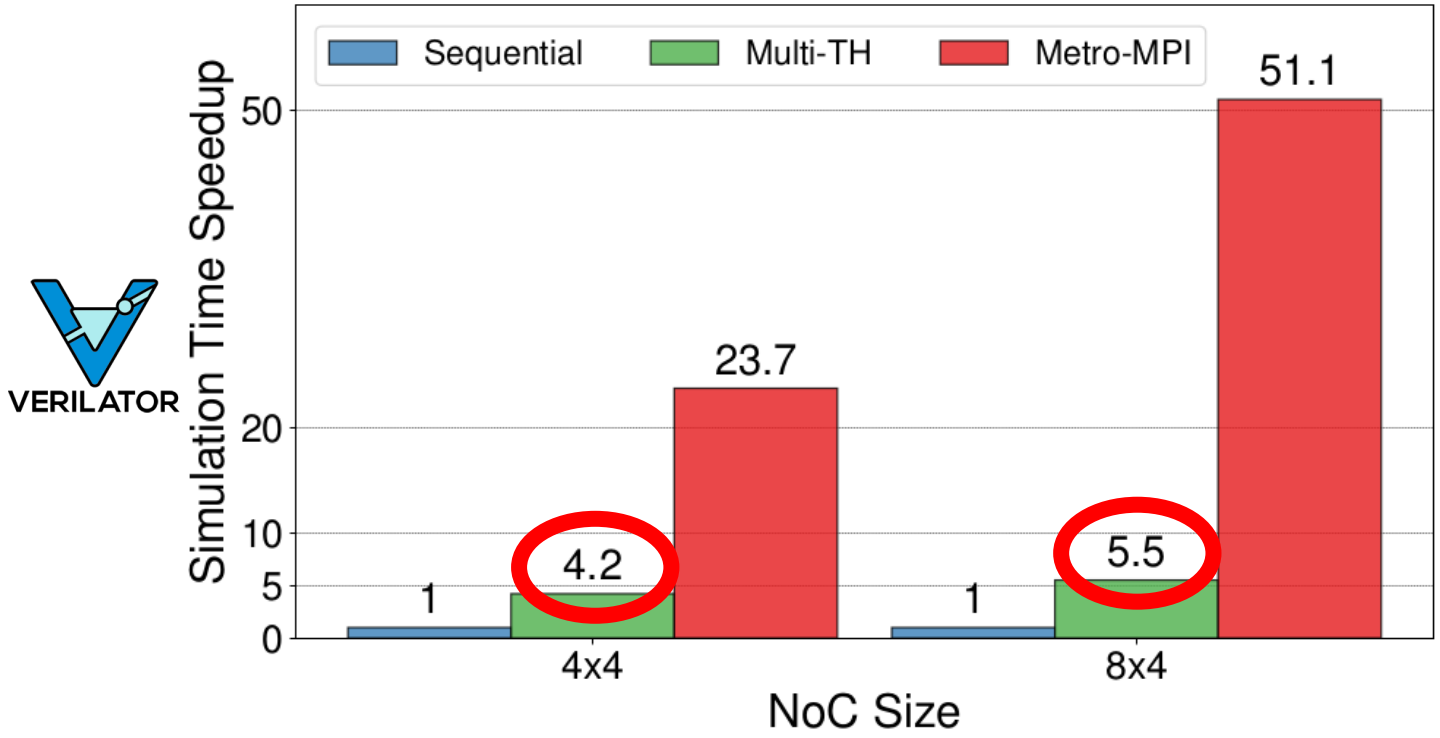

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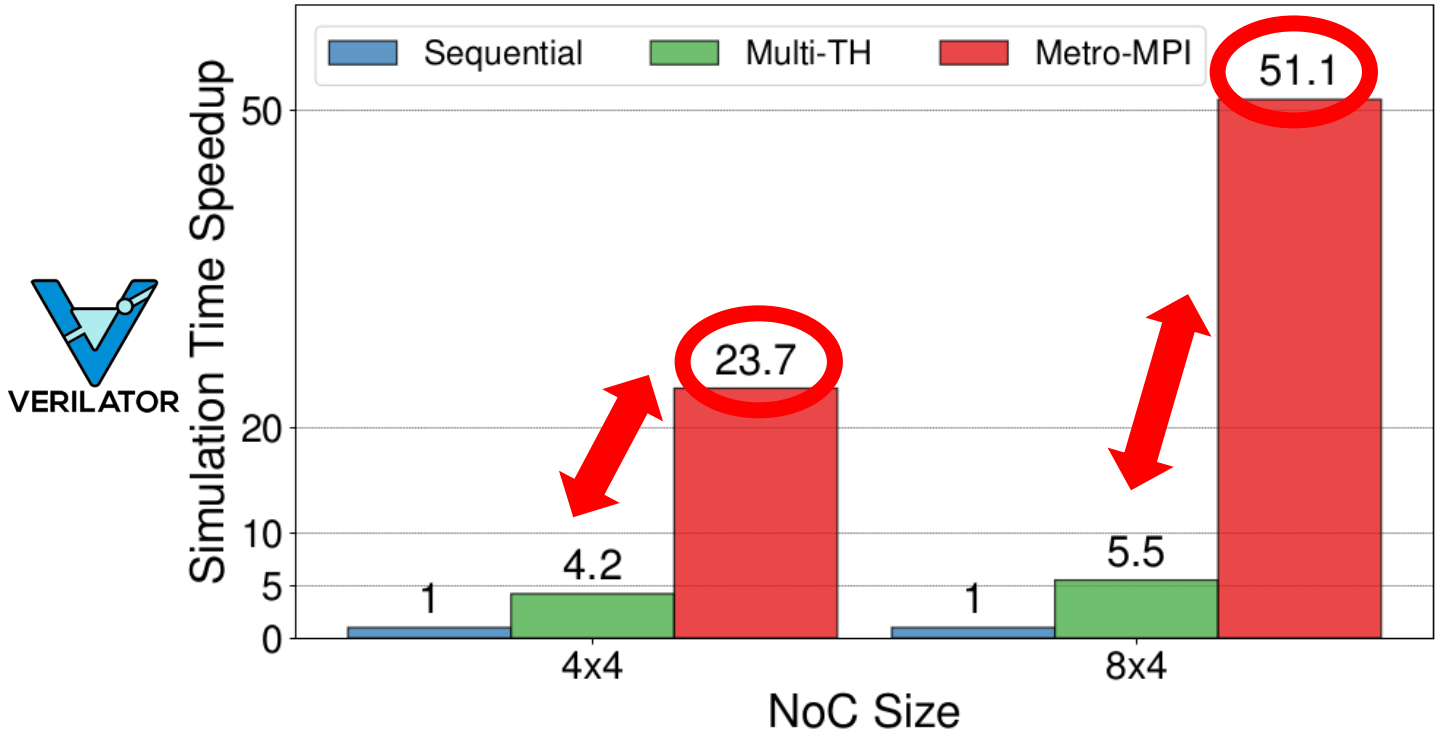

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- **We fix the amount of work (32 simulations of a 8x4 NoC Simulation) and compare three options**

- Metro-MPI outperforms in Time by 2.06x and 2.59x

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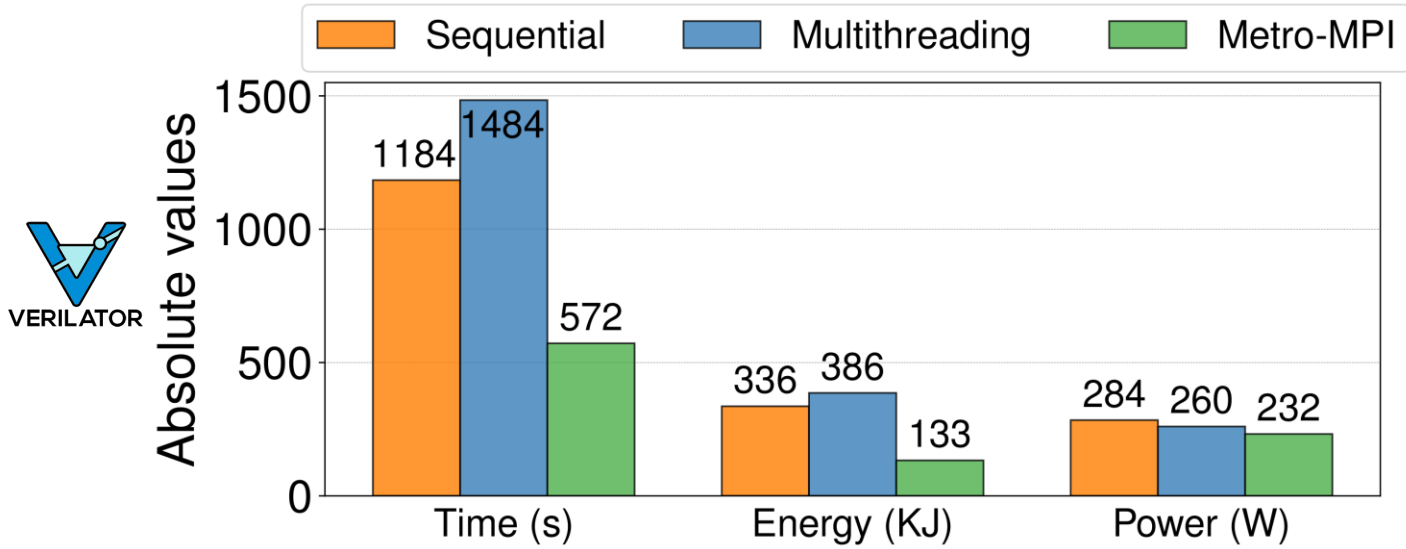

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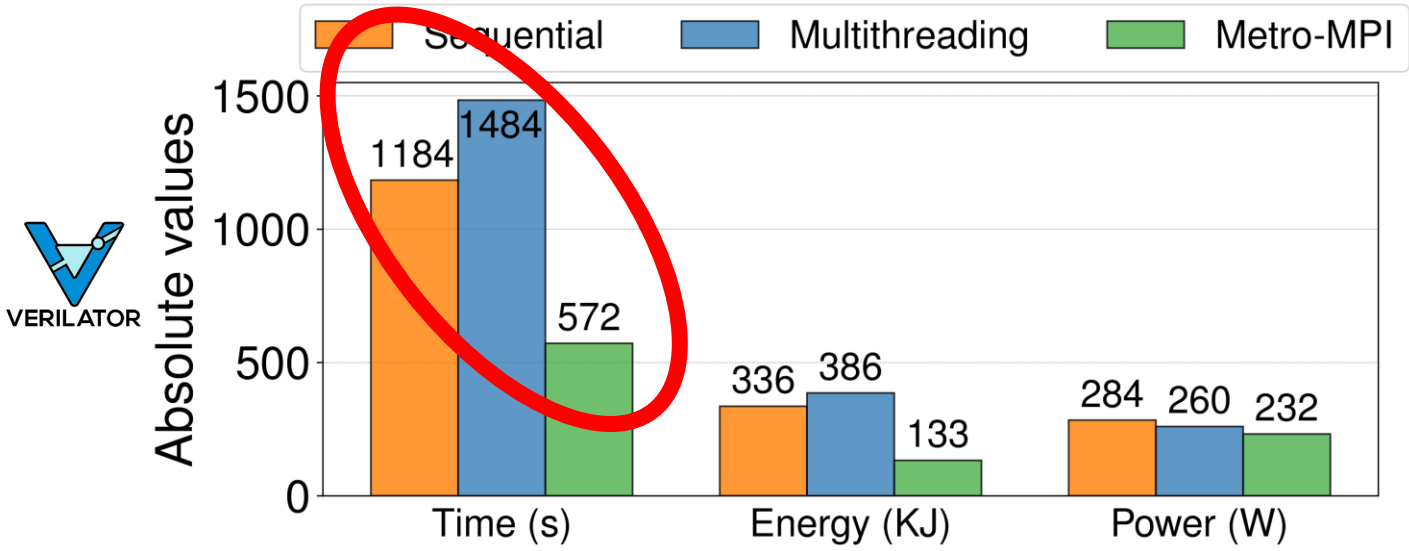

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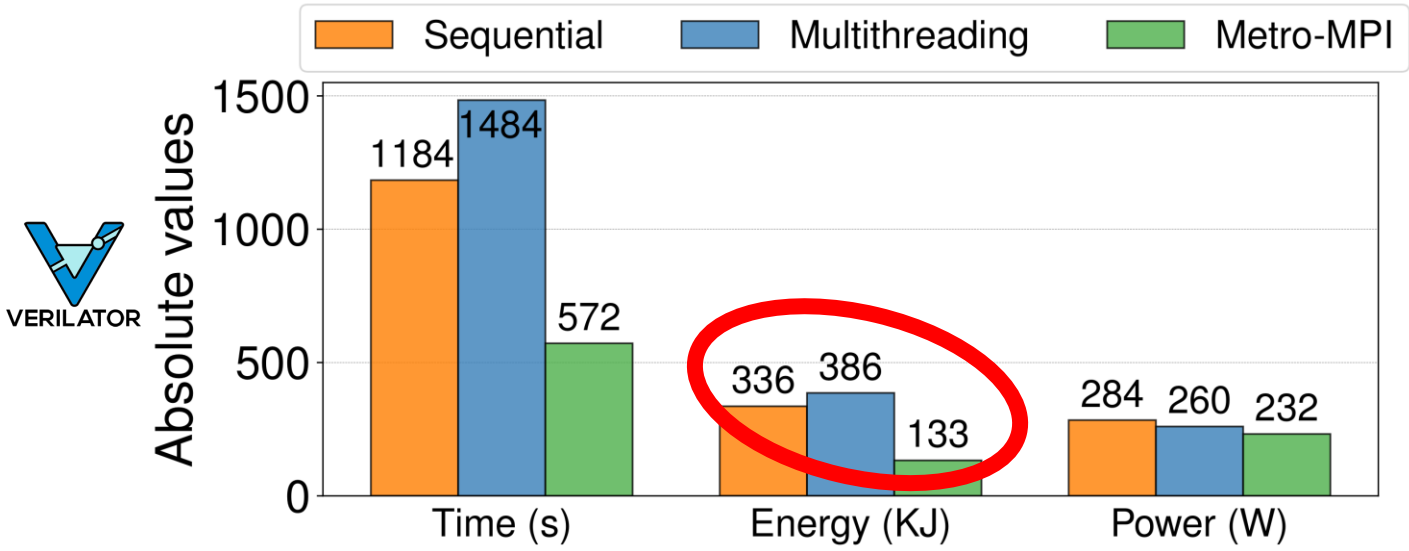

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- **Many projects at BSC working towards a heterogenous multi-core chip**

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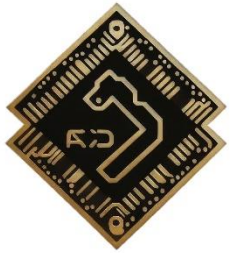

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- **Exceptional scaling:**
  - **Simulation scales up to 1024 tiles**
  - **In simulation throughput, reaching 2.7 MIPS on a 1024 tile chip**
  - **In simulation time speedup, up to 136x with respect to sequential**

Acknowledgments

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Google Summer of Code

DRAC

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HM

Metro-MPI

Open Source at: github.com/metro-mpi

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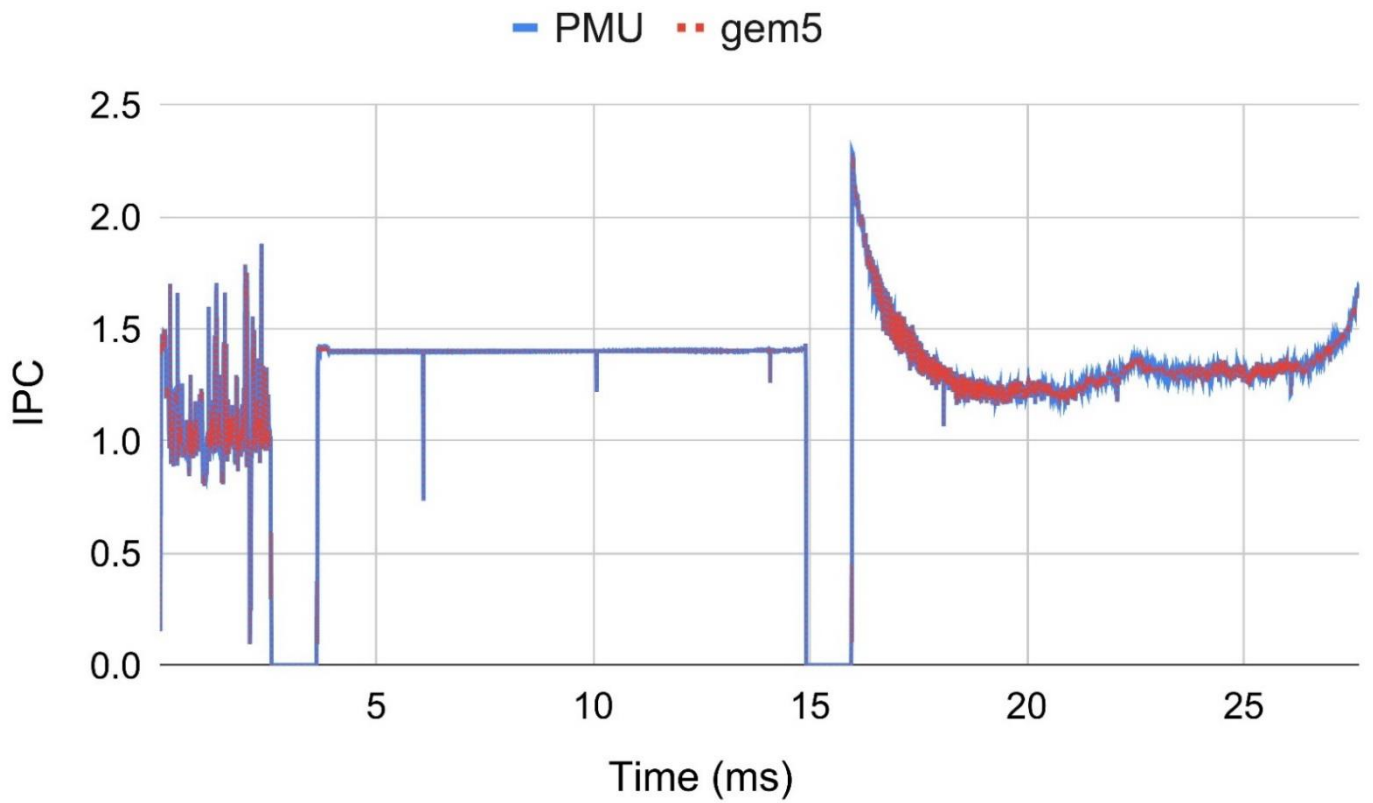

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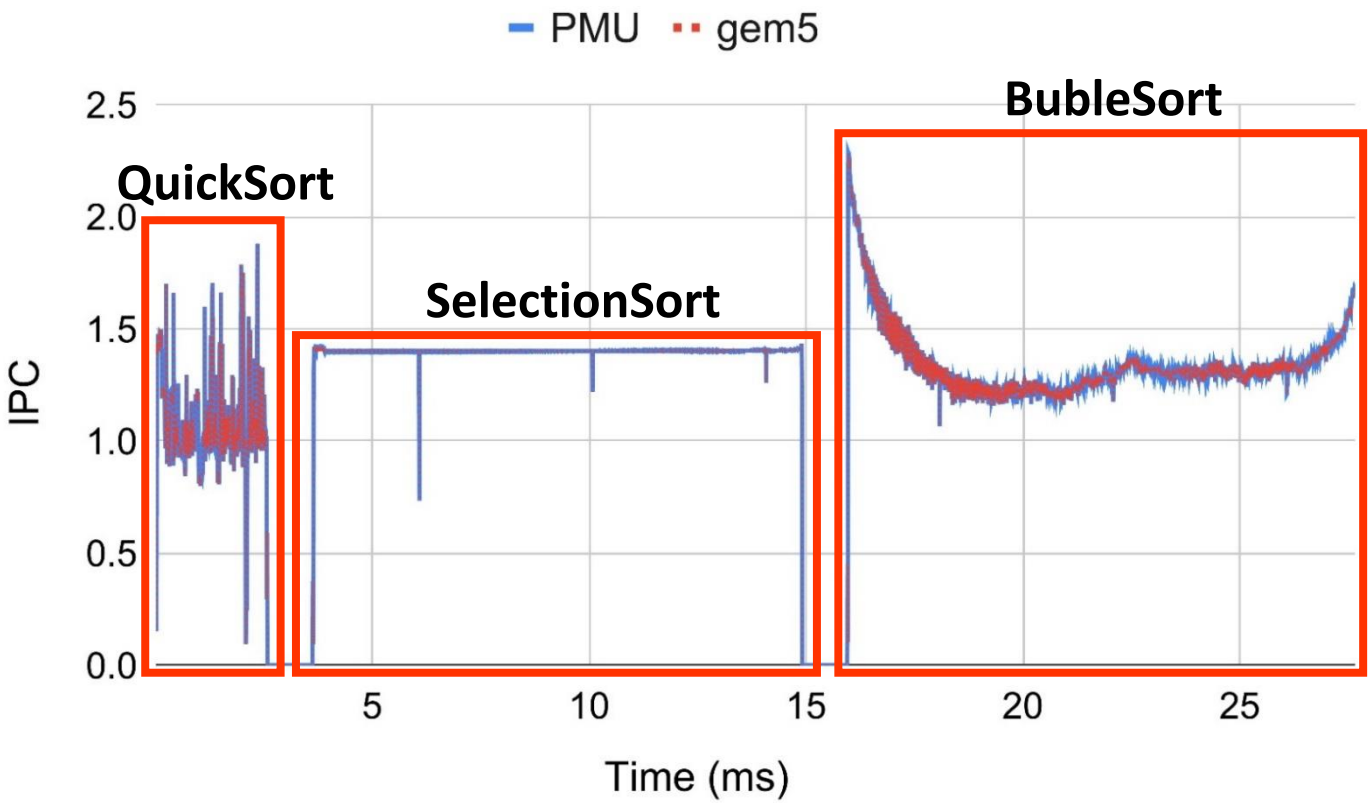

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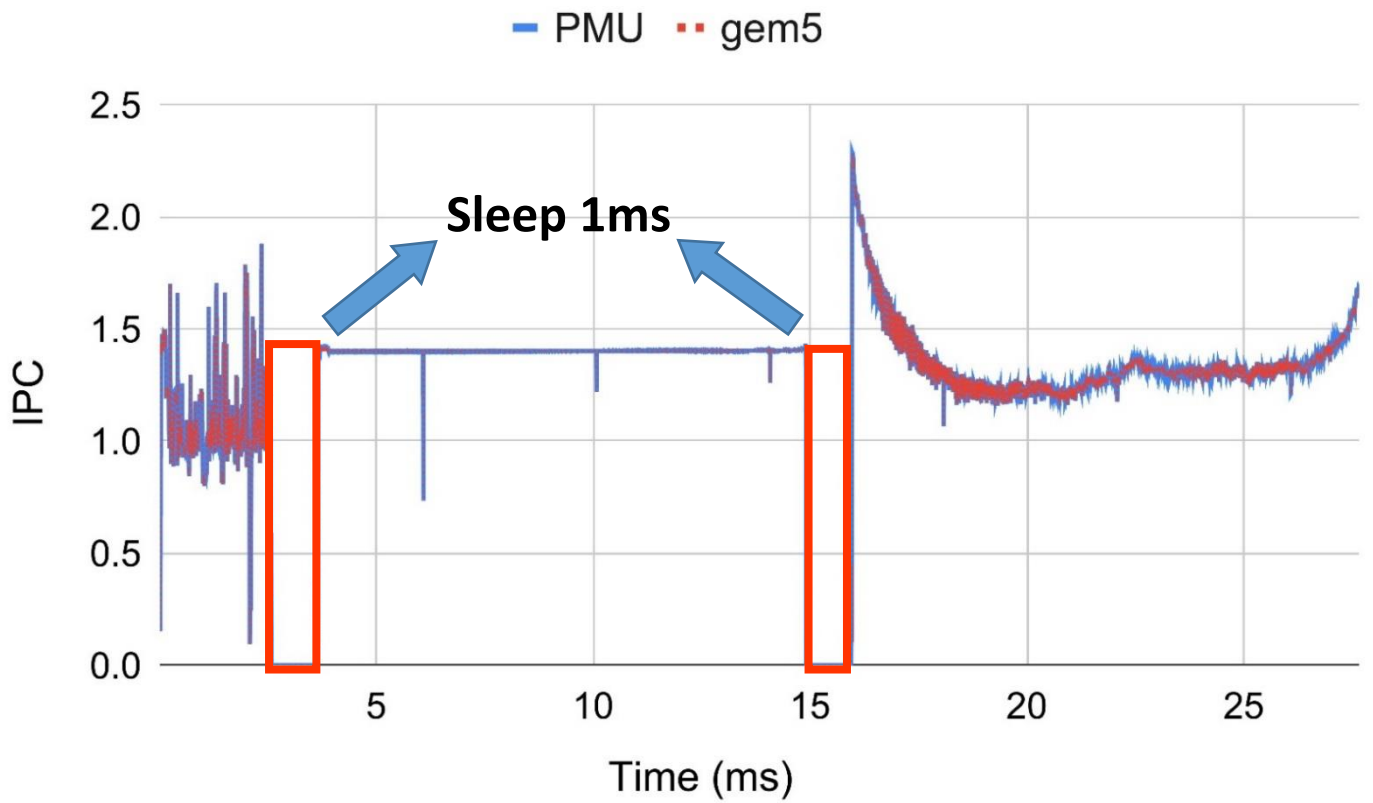

Evaluation NVDLA: GoogleNet

- **Evaluation of NVDLA performed by executing traces of real applications provided by NVIDIA**
- Parameters for the design space exploration (x-axis)
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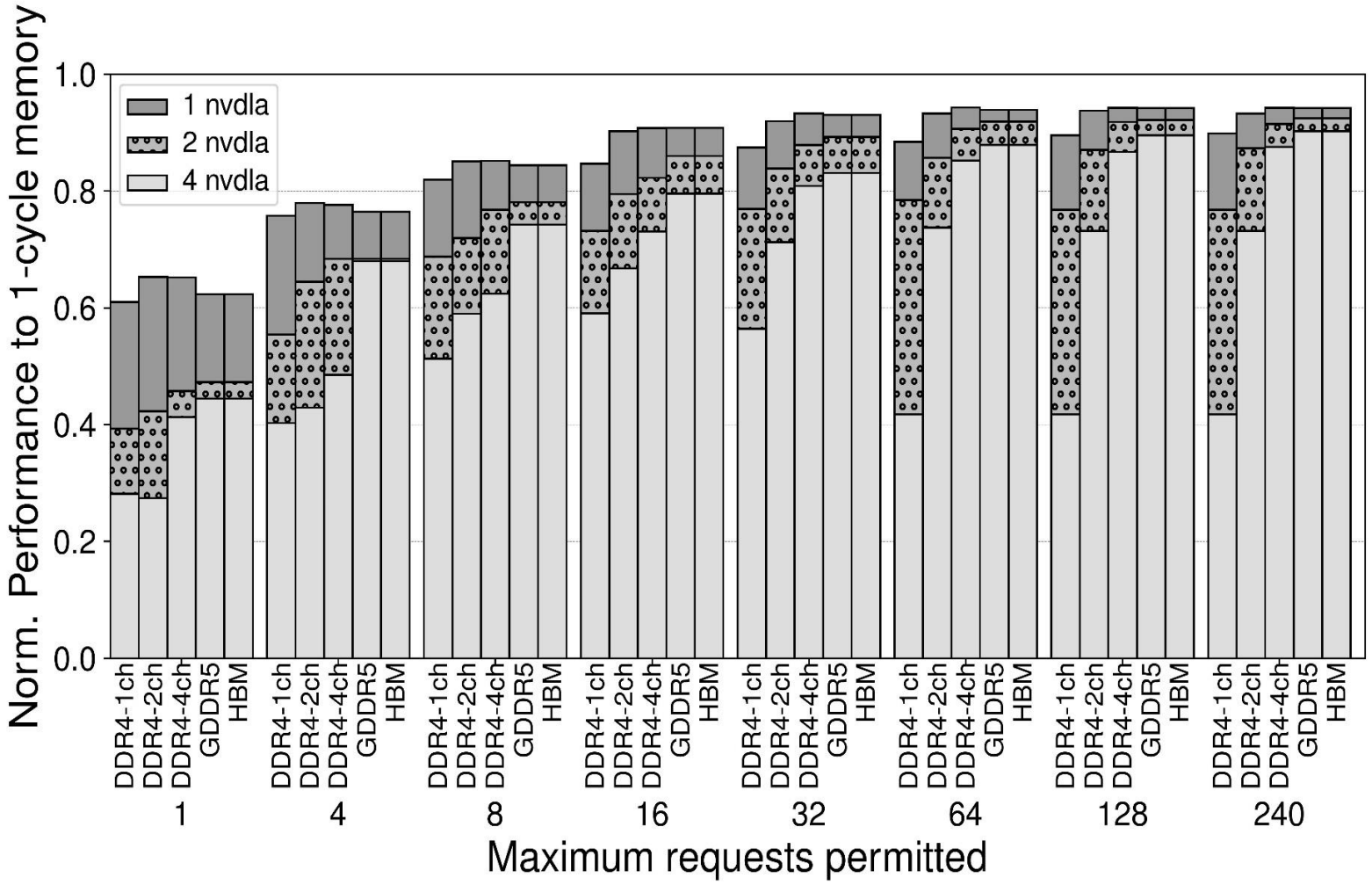

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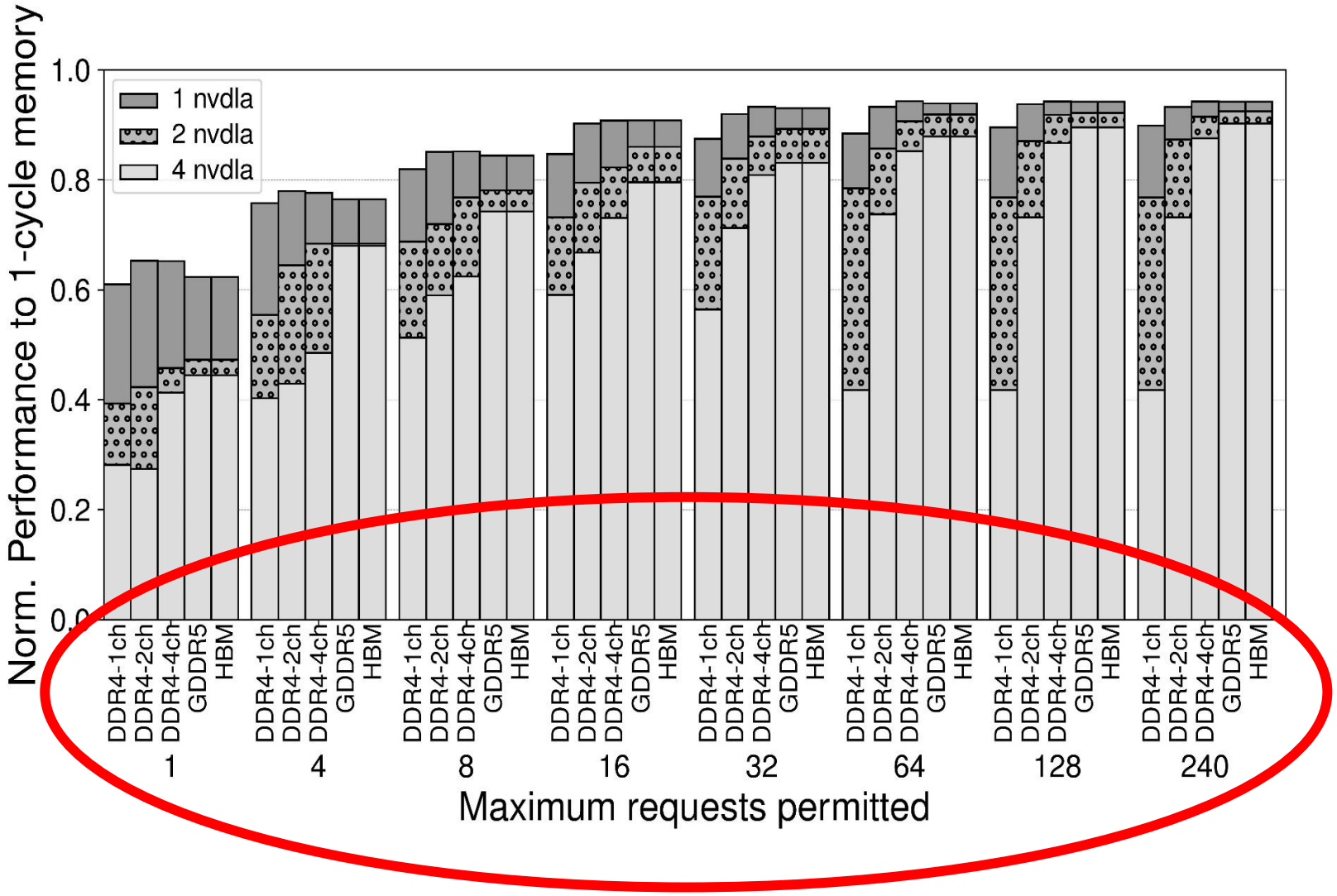

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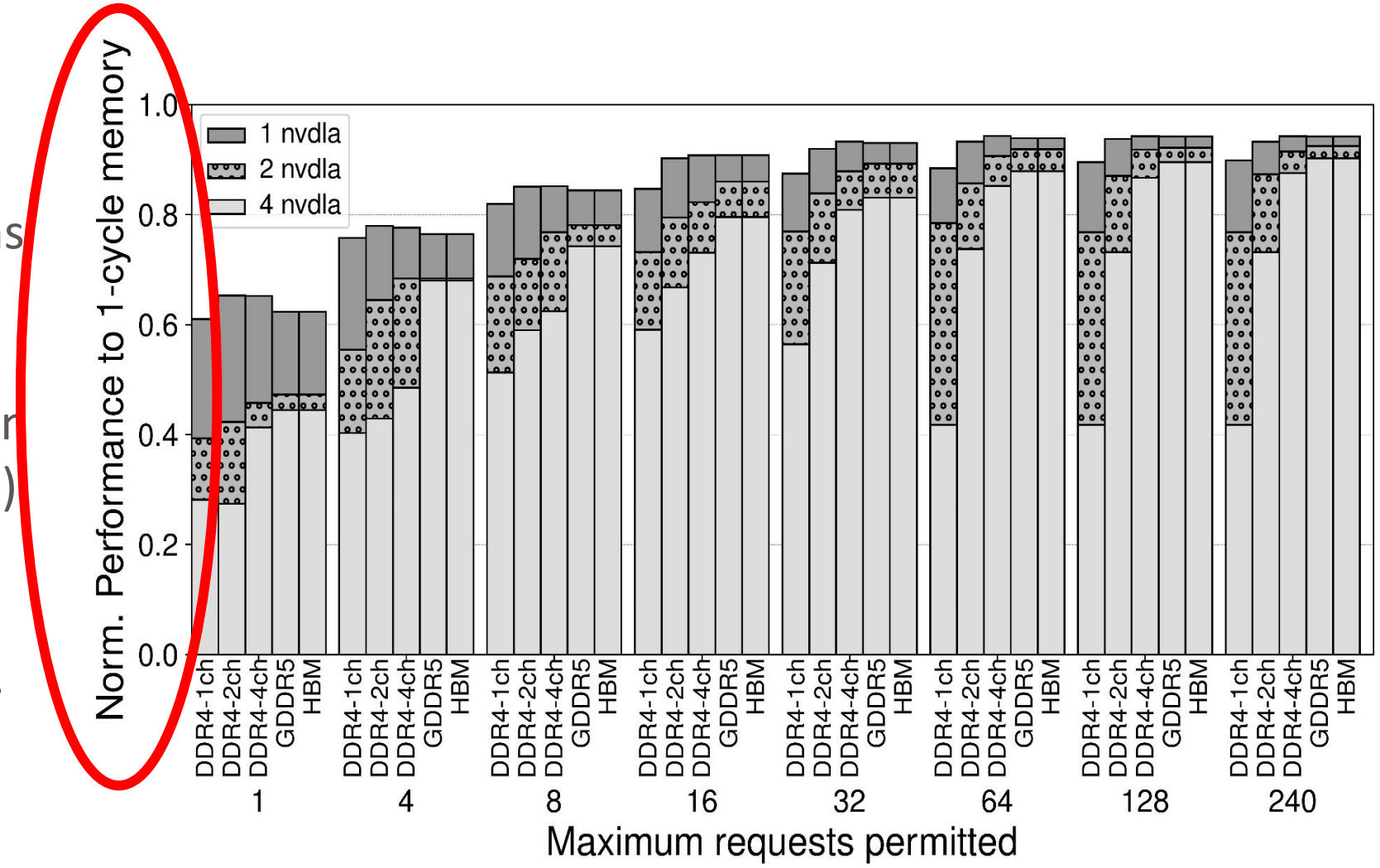
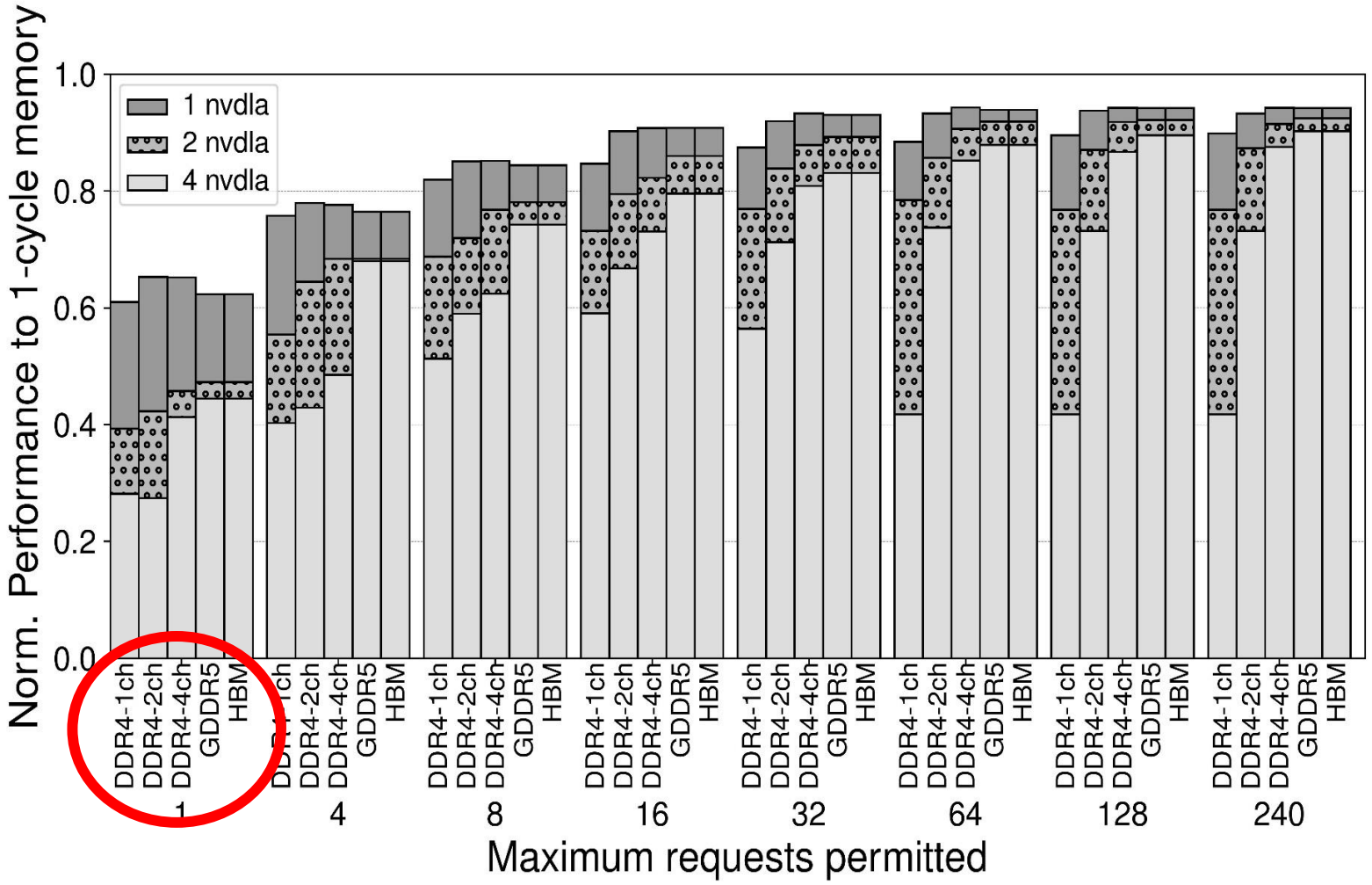


Evaluation NVDLA: GoogleNet

- **Using several memory configurations**
- Different number of maximum requests from NVDLA to main memory
- Different number of nvdla in the system: 1, 2 and 4 nvdla's configurations



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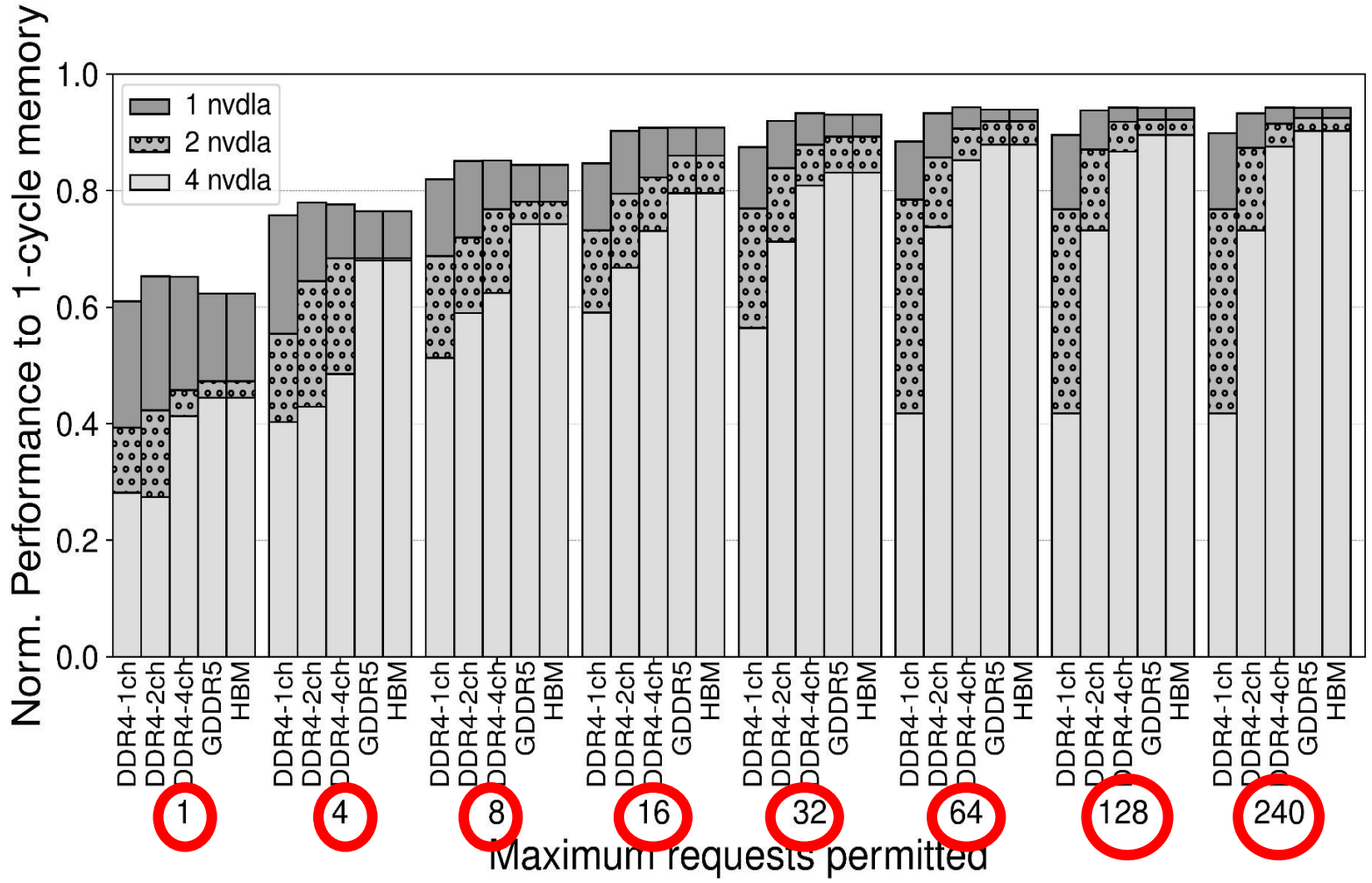

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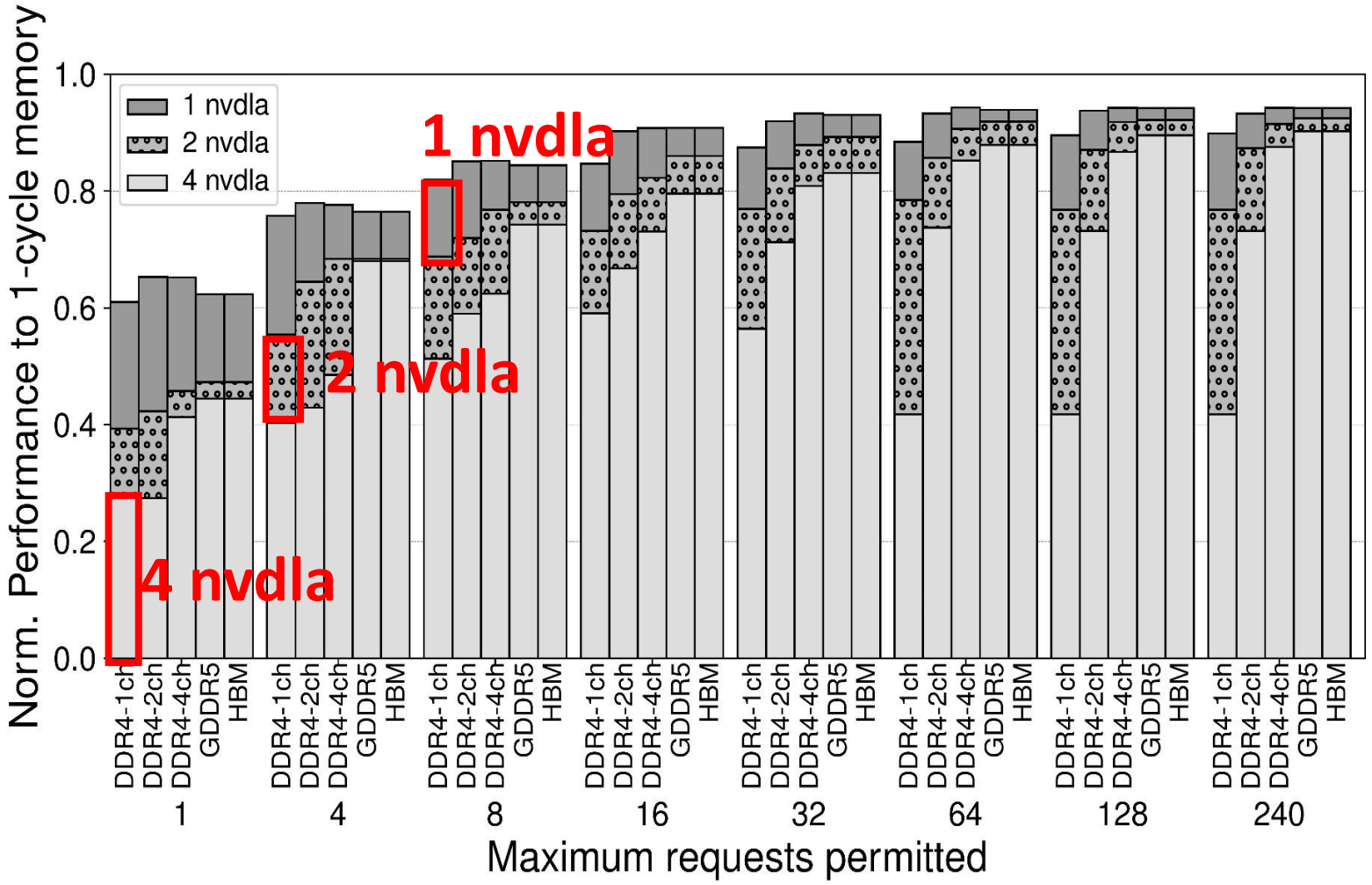
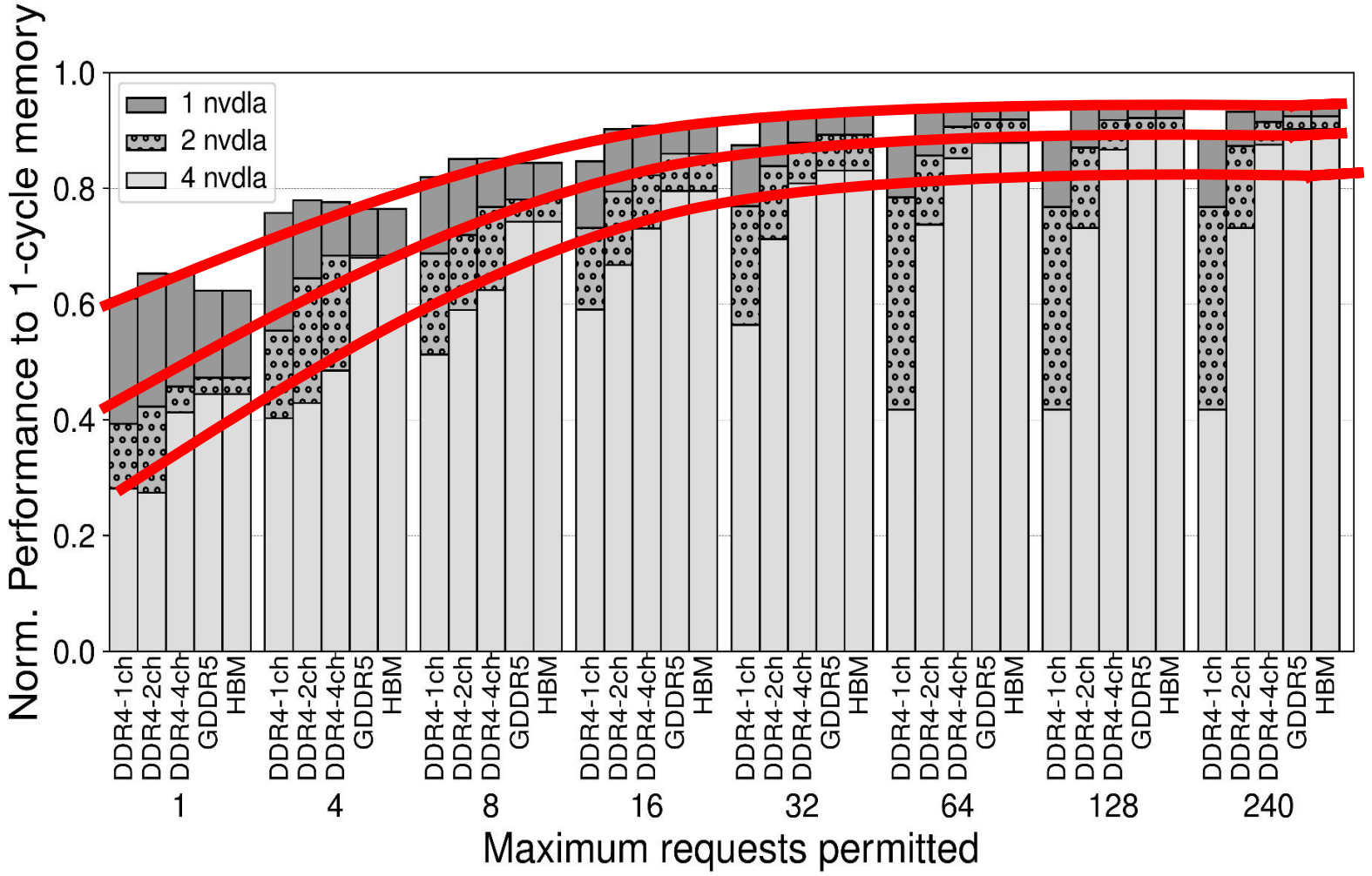


Evaluation NVDLA: GoogleNet

- **Maximum number of requests affects dramatically**
- Some memory configs cannot deliver enough bw for 2 and 4 nvdlas
- We recommend HBM or GDDR5 when more than 2 NVDLAs are in the system



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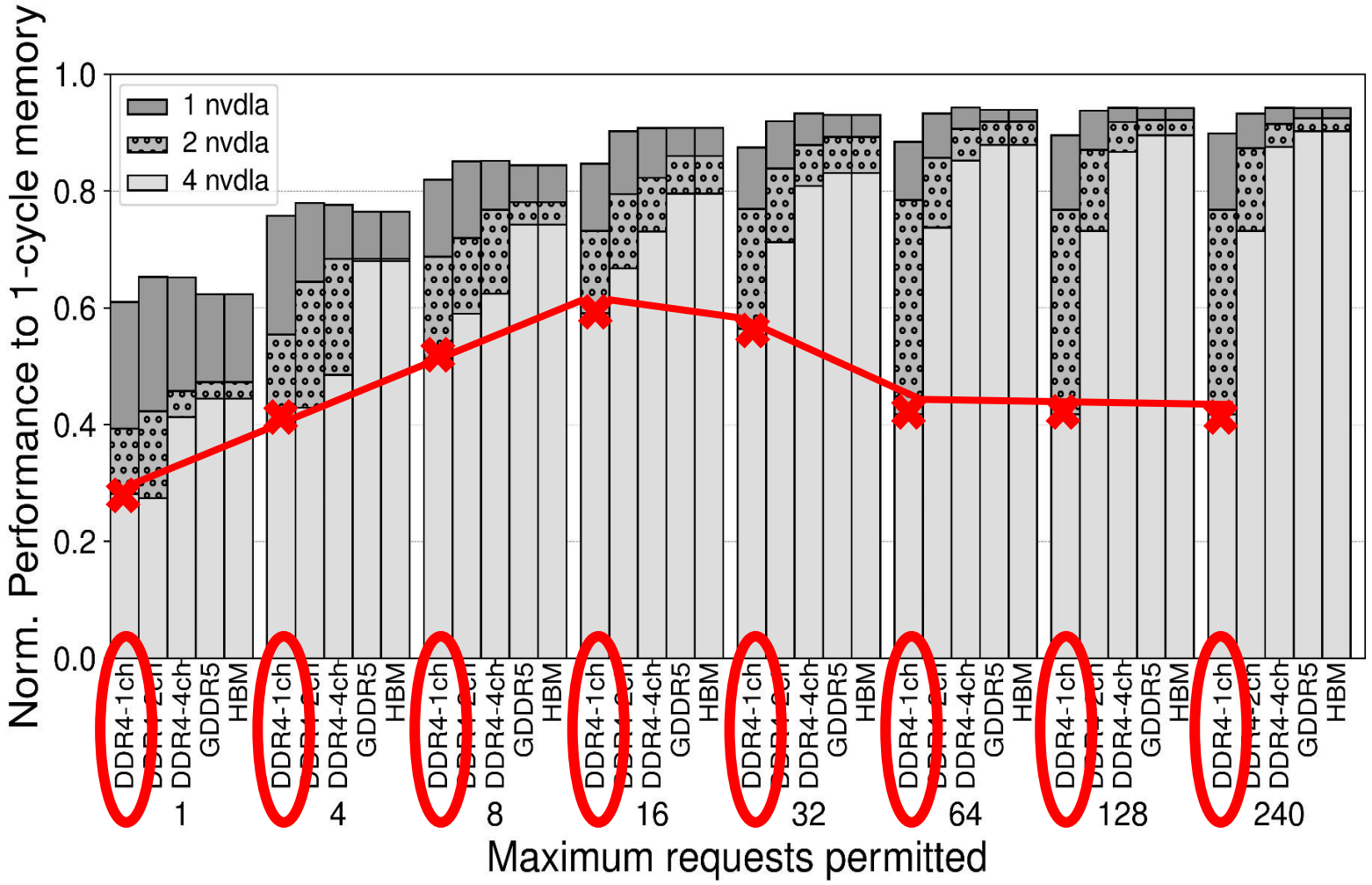
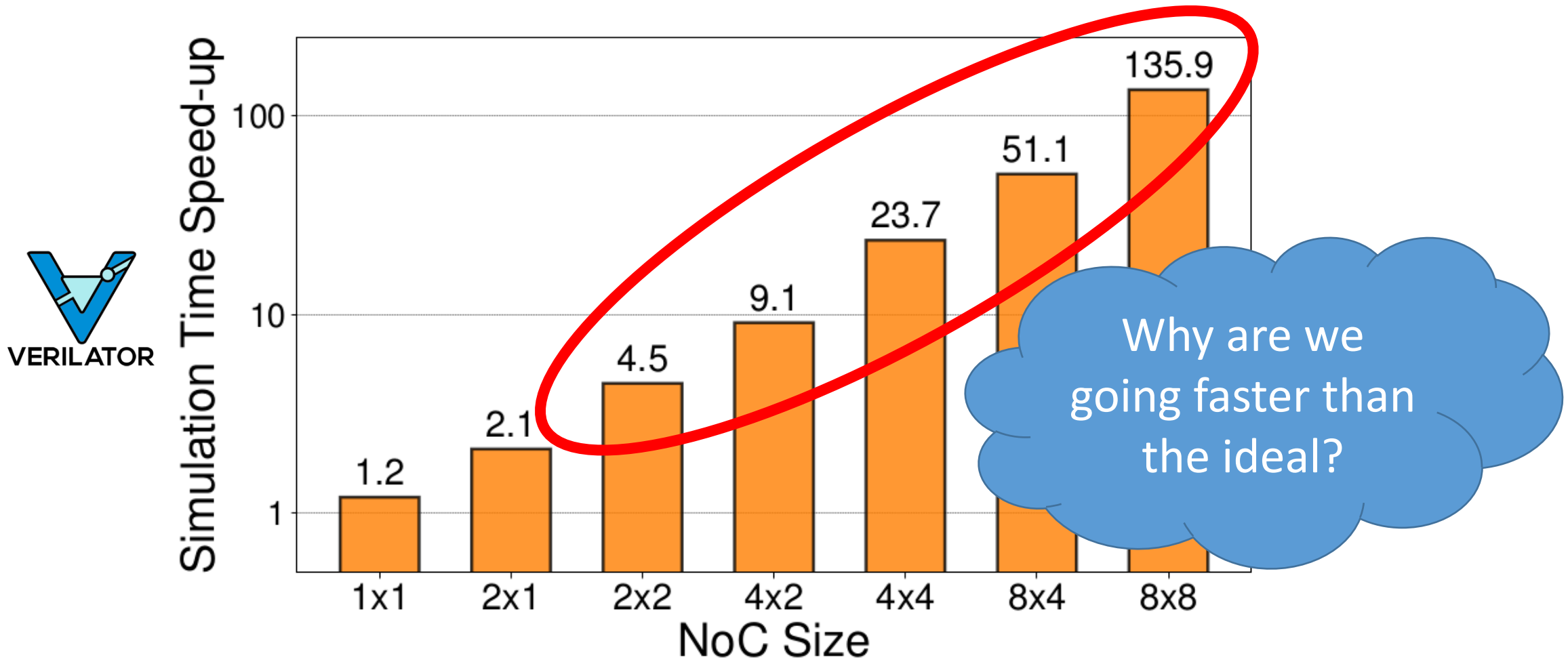
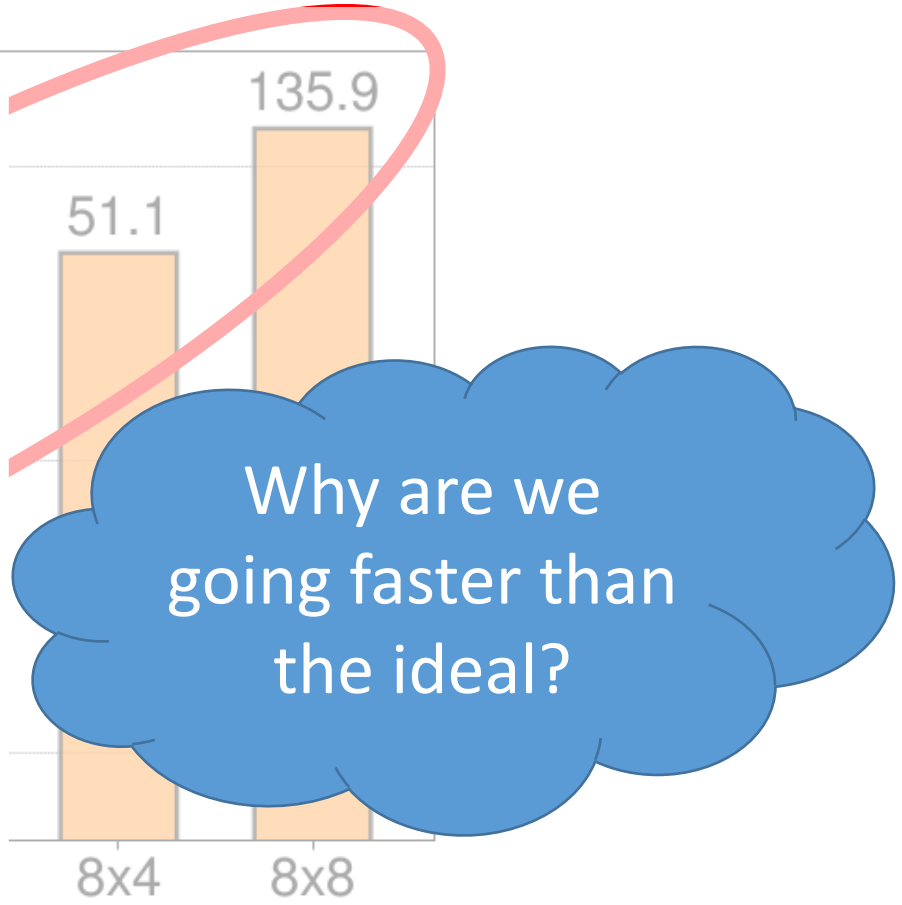


Metro-MPI Simulation Time Speedup



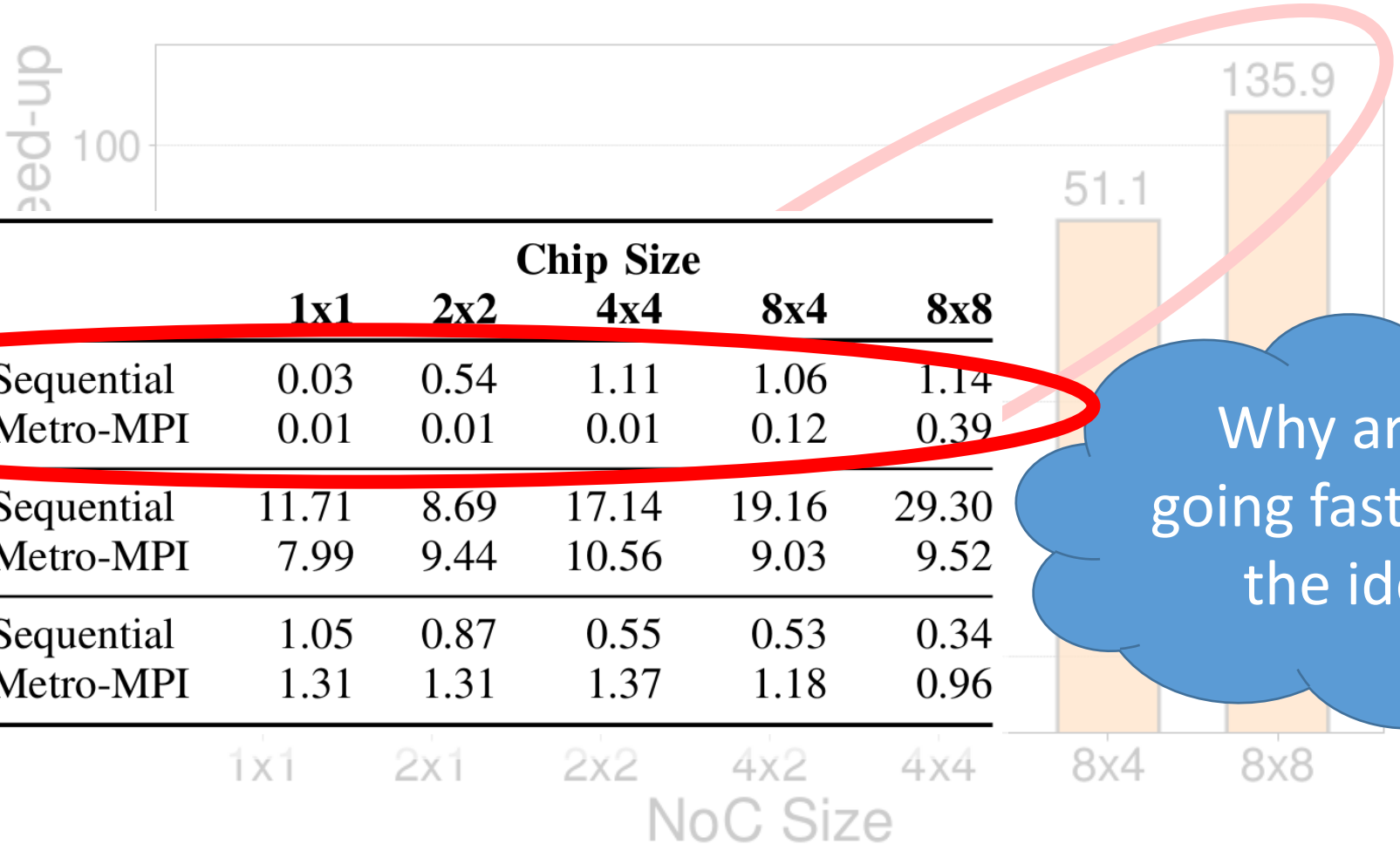
Metro-MPI Simulation Time Speedup

- **We did a Profiling Analysis**
  - **ITLB** Misses per 1k instr (**MPKI**)
  - **Icache** Misses per 1k instr (**MPKI**)
  - **IPC**



Metro-MPI Simulation Time Speedup

		Chip Size 1x1	2x2	4x4	8x4	8x8
ITLB MPKI	Sequential	0.03	0.54	1.11	1.06	1.14
	Metro-MPI	0.01	0.01	0.01	0.12	0.39
ICache MPKI	Sequential	11.71	8.69	17.14	19.16	29.30
	Metro-MPI	7.99	9.44	10.56	9.03	9.52
IPC	Sequential	1.05	0.87	0.55	0.53	0.34
	Metro-MPI	1.31	1.31	1.37	1.18	0.96



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Metro-MPI Big-3 Performance

- In a system with 8 cores
- Big 3 Simulator scales almost linearly
- Big 3 is already using threads in the default (non metro-MPI version)

TABLE III: Metro-MPI scaling with a commercial simulator.

Speedups	1x1	2x1	2x2	4x2	4x4	8x4
Simulation time	0.93	1.54	3.20	6.17	8.44	7.81
CPS	0.91	1.26	2.73	5.15	7.08	6.75
IPS	1.41	1.36	2.82	5.36	7.35	6.90

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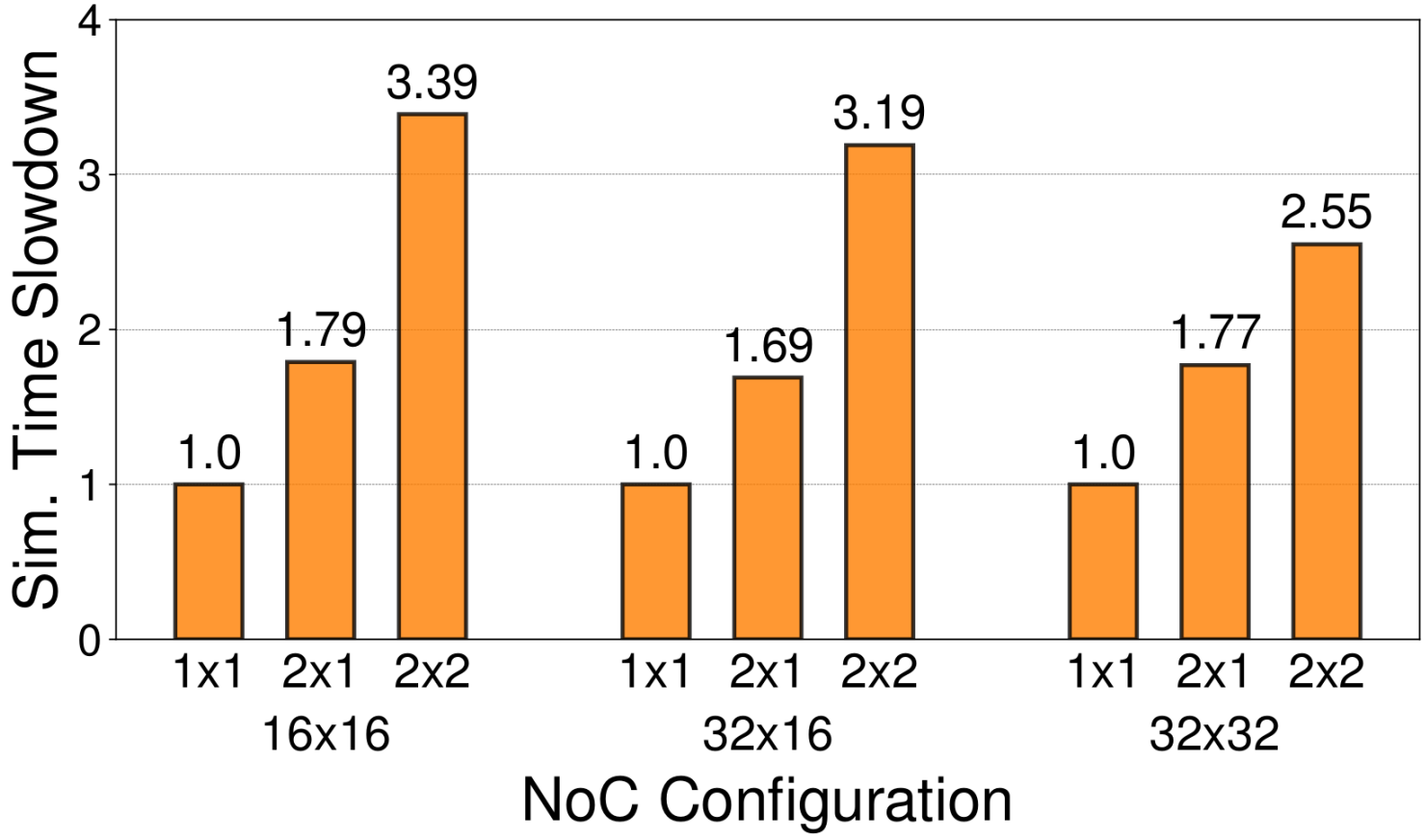
Multi Tile Granule Performance

- **Slow-down in simulation time**
- Consequently, KIPS also slow downs
- But, work per core increases, hence to run regressions is better ☺



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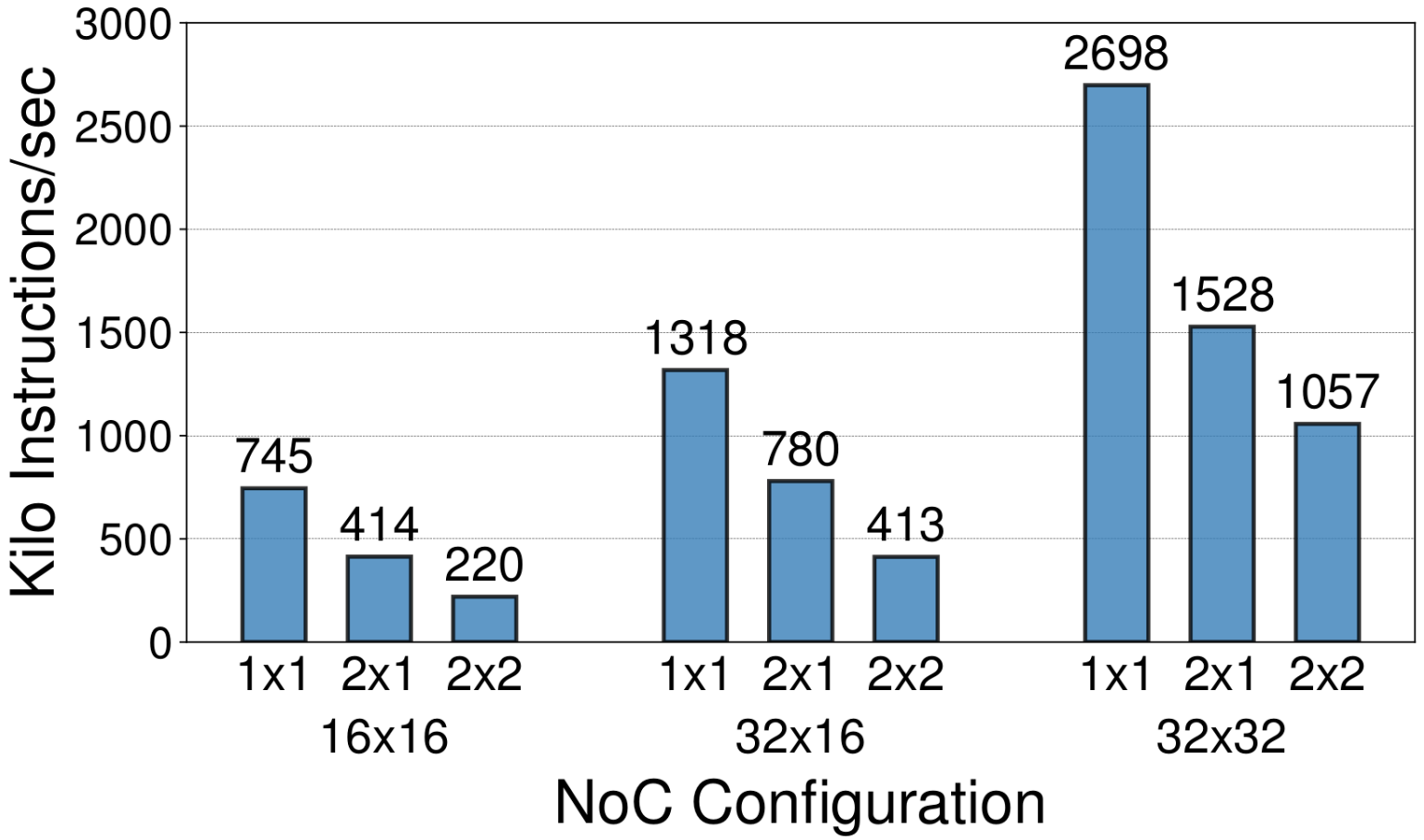

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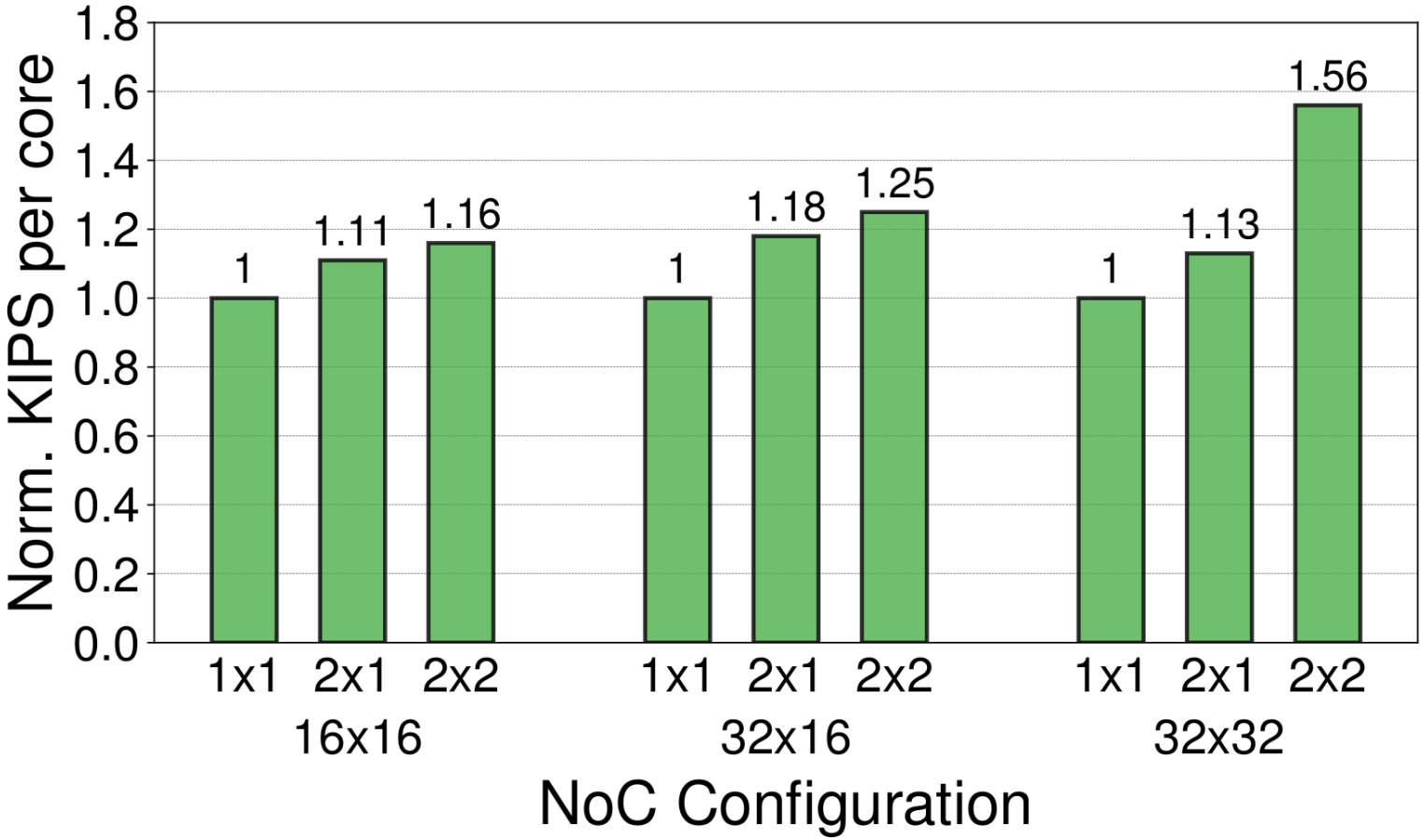
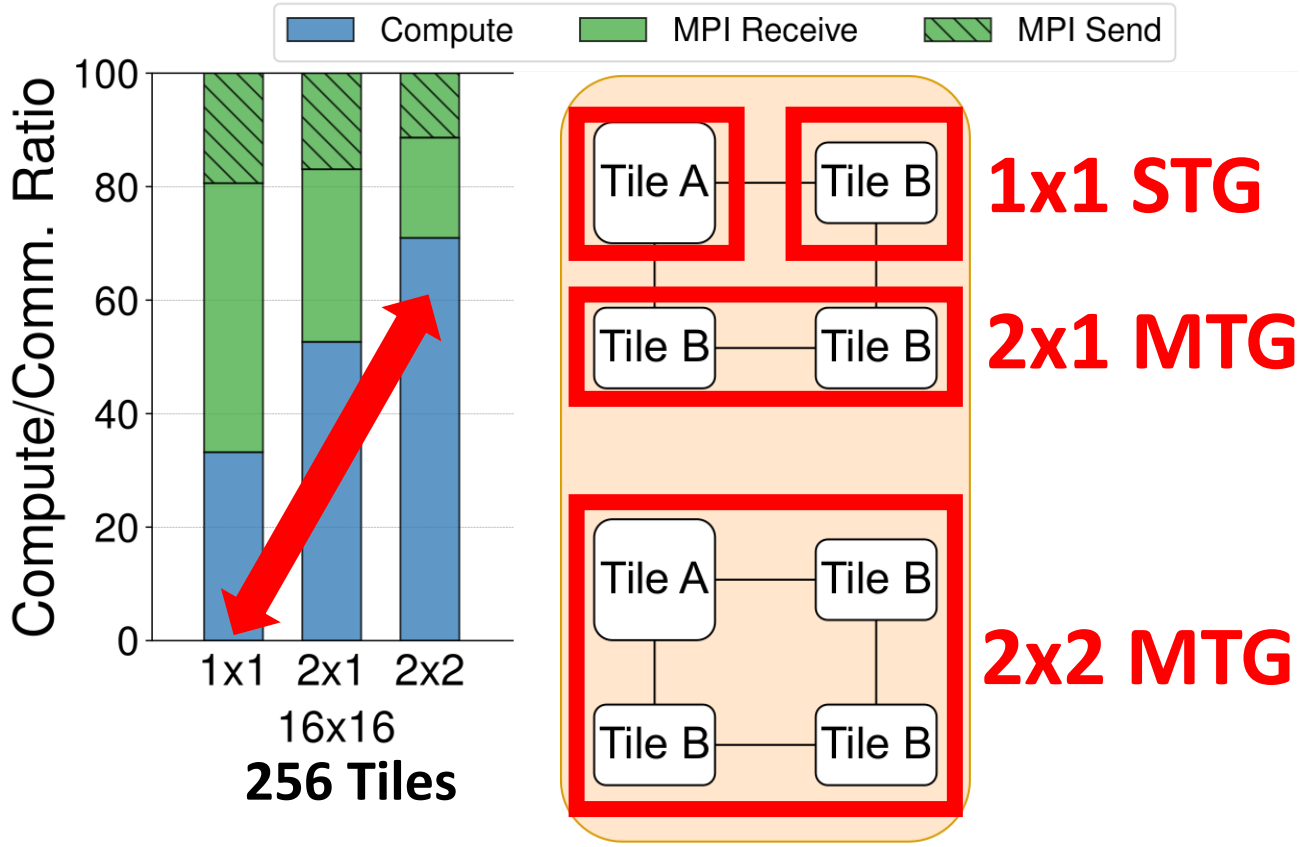


MPI Overhead (Multi Tile)

- **Multi-Tile granules (MTG) help to increase the compute ratio**



MPI Overhead (Multi Tile)

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- **MPI Receive decreases as the number of MPI processes is reduced**