All Open Source Toolchain for ZYNQ 7000 SoCs

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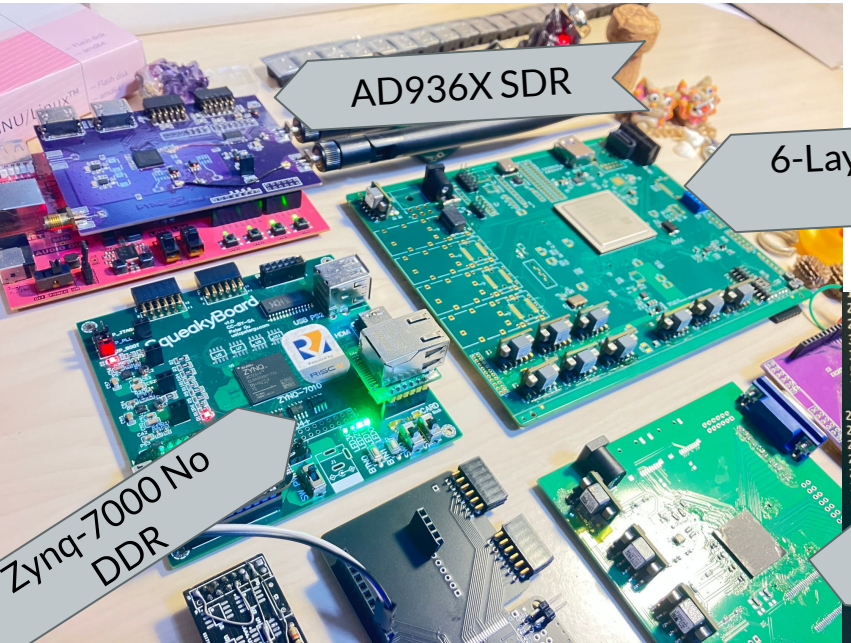
Symbiotic EDA
OSCAR 2025

About Me

- PhD candidate @ U-Tokyo
- Amateur FPGA programming, RISC-V,
  PCB design, ZYNQ, Maker Faire, etc

Hackers & Painters

I'm neither



MMU/No-MMU 32-bit RISC-V SoC

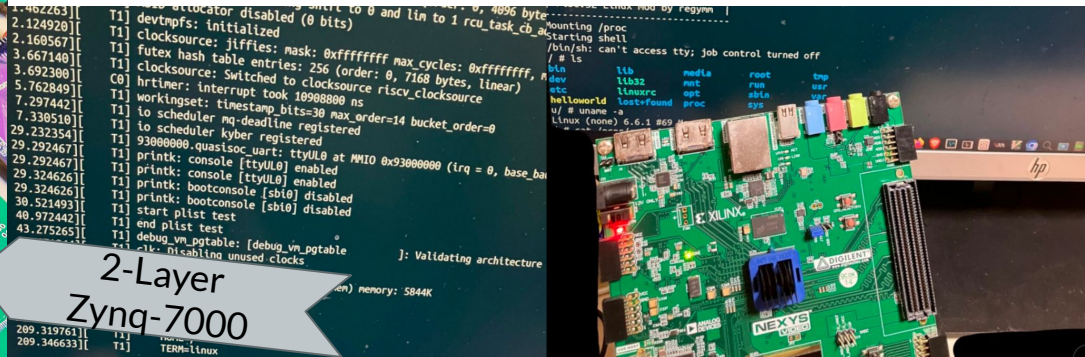


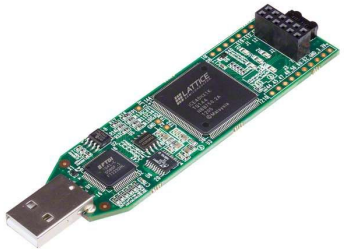
Table of Contents

Open-source FPGA Toolchains

From iCE40 to Kintex 7

- Icestorm for **Lattice iCE40**, in 2015
- PrjTrellis for **Lattice ECP5**
- Project Apicula 🐝 for **Gowin**
- F4PGA for **Xilinx 7 Series**
- OpenXC7 supports **Kintex 7**

- ice40hx8k, 8K LE
- lfe5u-85f, 85K LE
- gw2ar, 20K LE
- xc7a200t, 200K LE
- xc7k480t, 480K LE



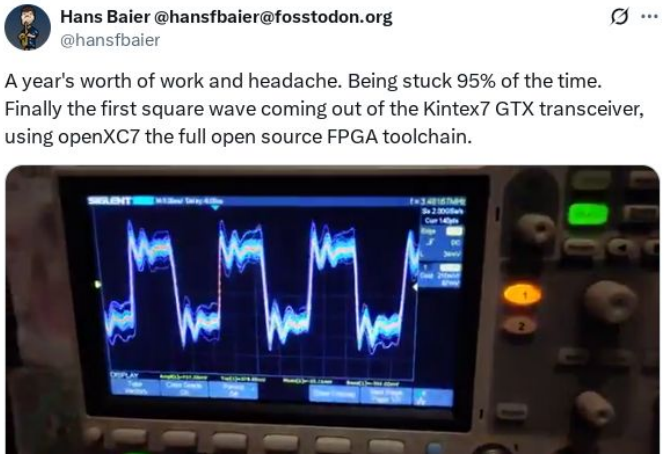
Possibilities

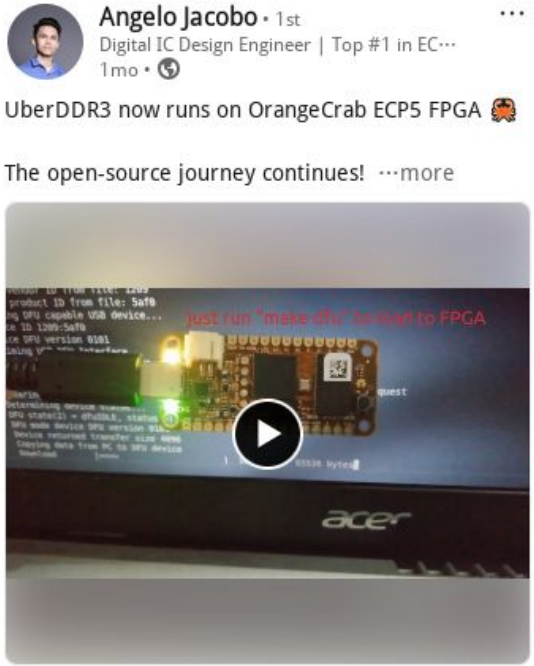
- PicoRV32, UberDDR3, Quasi SoC (No-MMU), KianRiscV, SD Card, HDMI, MMCM, IOSERDES
- Spartan 7/Artix 7/Kintex 7, **Zynq 7000 PL, GTP, Artix 7 PCIe**
- SATA controller, 10G ETH, GTX, PCIe Root Complex softcore

Runs on ARM Machines

(Apple M1 included)

Runs in Docker





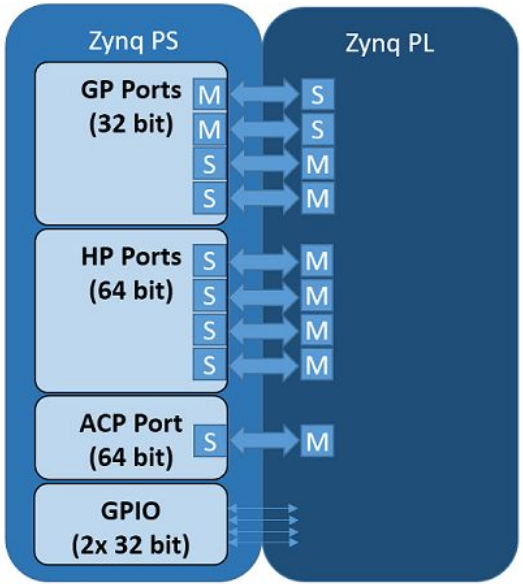
Now Zynq!

Double trouble?

- “Unique” PS + PL structure

2x ARM A9, DDR3
ETH/USB/…
Flexible pins
Boot

Linux / RTOS



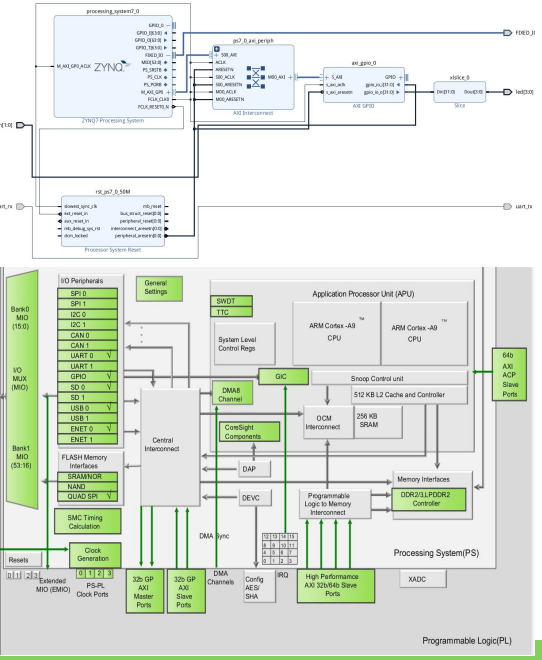
FPGA fabric,
HDMI/ETH/LED/…

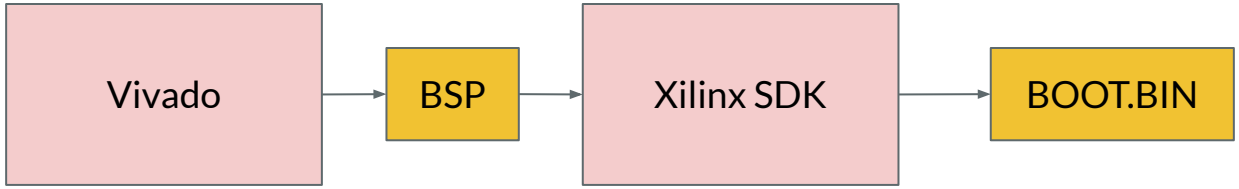
Custom Logic
bitstream

https://pynq.readthedocs.io/en/latest/overlay_design_methodology/pspl_interface.html

Are you confident…

- Building a Zynq BOOT.BIN firmware by yourself?
- How long does it take?





.bit

PL Bitstream
PS Configuration

ps7_init.c
xparameters.h

FSBL
User App

.bit

fsbl.elf
UserApp.elf

Hundreds of mouse clicks!

Decoding the ARM registers

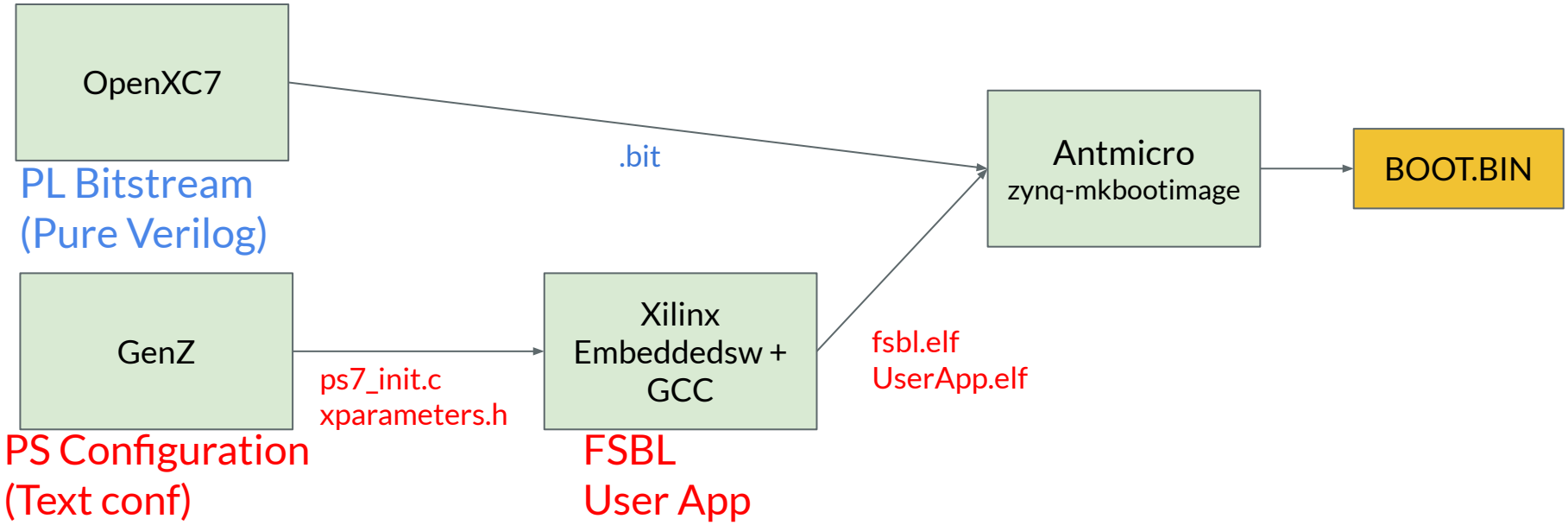
- 100+ reg writes
- Zynq 7000 SoC Technical Reference Manual (UG585)
  - PLLs
  - Clock Freqs
  - DDR (TODO)
  - MIO MUXs
  - Peripherals
  - Debug (???)

ps7_init.c

```
// START: top
// .. START: SLCR SETTINGS
// .. UNLOCK_KEY = 0XDF0D
// .. ==> 0XF8000008[15:0] = 0x0000DF0DU
// ..      ==> MASK : 0x0000FFFFU    VAL : 0x0000DF0DU
// ..
EMIT_WRITE(0XF8000008, 0x0000DF0DU),
// .. FINISH: SLCR SETTINGS
// .. START: PLL SLCR REGISTERS
// .. .. START: ARM PLL INIT
// .. .. PLL_RES = 0x2
// .. .. ==> 0XF8000110[7:4] = 0x00000002U
// .. ..      ==> MASK : 0x000000F0U    VAL : 0x00000020U
// .. .. PLL_CP = 0x2
// .. .. ==> 0XF8000110[11:8] = 0x00000002U
// .. ..      ==> MASK : 0x00000F00U    VAL : 0x00000200U
// .. .. LOCK_CNT = 0xfa
// .. .. ==> 0XF8000110[21:12] = 0x000000FAU
// .. ..      ==> MASK : 0x003FF000U    VAL : 0x000FA000U
// .. ..
EMIT_MASKWRITE(0XF8000110, 0x003FFFF0U ,0x000FA220U),
// .. .. .. START: UPDATE FB_DIV
// .. .. .. PLL_FDIV = 0x28
// .. .. .. ==> 0XF8000100[18:12] = 0x00000028U
// .. .. ..      ==> MASK : 0x0007F000U    VAL : 0x00028000U
// .. .. ..
EMIT_MASKWRITE(0XF8000100, 0x0007F000U ,0x00028000U),
// .. .. .. FINISH: UPDATE FB_DIV
// .. .. .. START: BY PASS PLL
// .. .. .. PLL_BYPASS_FORCE = 1
// .. .. .. ==> 0XF8000100[4:4] = 0x00000001U
// .. .. ..      ==> MASK : 0x00000010U    VAL : 0x00000010U
// .. .. ..
EMIT_MASKWRITE(0XF8000100, 0x00000010U ,0x00000010U),
// .. .. .. FINISH: BY PASS PLL
// .. .. .. START: ASSERT RESET
// .. .. .. PLL_RESET = 1
// .. .. .. ==> 0XF8000100[0:0] = 0x00000001U
// .. .. ..      ==> MASK : 0x00000001U    VAL : 0x00000001U
```

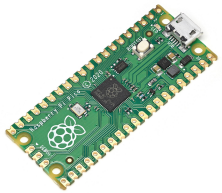
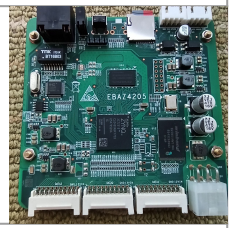
OpenXC7 + GenZ

- BOOT.BIN in **5 minutes**
- Awesome through 2035



What does this mean?

Enjoy RP2040? How about Zynq!

	RP2040	**Zynq 7010**
“PS”	2x Cortex M0+ @ 133 MHz 264 kB SRAM UART, SPI, etc USB 1.1 	2x Cortex A9 @ 667 MHz 256 kB OCM + DDR UART, SPI, SDCARD, etc USB 2.0, 1Gbps ETH 
“PL”	8x Programmable I/Os Modules	28K+ LE
I/O	30 GPIOs	80+ HR I/Os
Price	<€5	€10 - €200
Toolchain	**Cross platform, FOSS** pico-sdk-2.1.0.tar.gz 2.3 MB Nov 25, 2024	**x86 Win/Linux only, Proprietary** Vivado HLx 2019.1: All OS installer Single-File Download (TAR/GZIP - 21.39 GB) **U.S. Government Export Approval**

Enjoy RP2040? How about Zynq!

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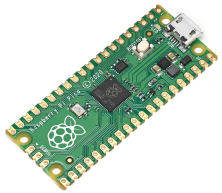
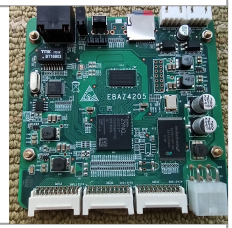
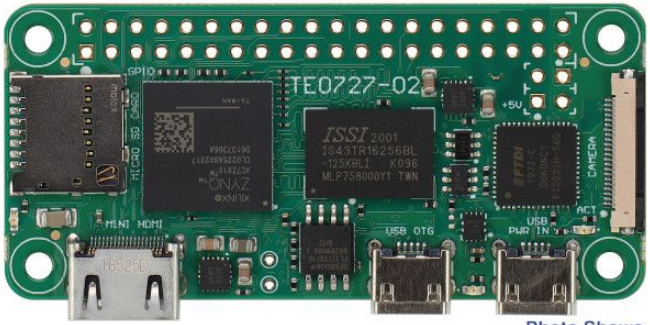
“PS”	2x Cortex M0+ @ 133 MHz 264 kB SRAM UART, SPI, etc USB 1.1 	2x Cortex A9 @ 667 MHz 256 kB OCM + DDR UART, SPI, SDCARD, etc USB 2.0, 1Gbps ETH 
“PL”	8x Programmable I/Os Modules	28K+ LE
I/O	30 GPIOs	80+ HR I/Os
Price	<€5	€10, €60 - €200
Toolchain	**Cross platform, FOSS** pico-sdk-2.1.0.tar.gz 2.3 MB Nov 25, 2024	**Cross platform, FOSS** **docker pull regymm/openxc7** **git clone https://.../GenZ**

Zynq-as-MCU

- Boards are available
- Upcycled boards set price at **€10**

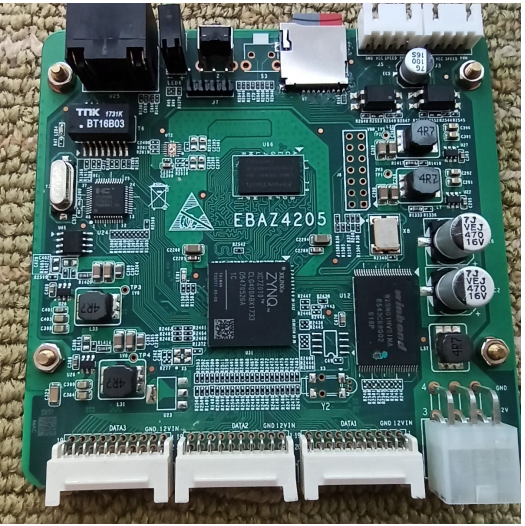


shop.trenz-electronic.de

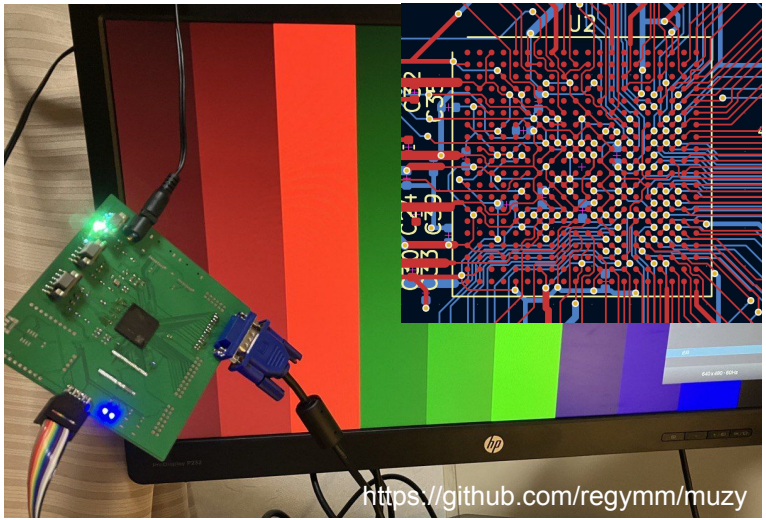
Photo Shows Similar Product

ZynqBerryZero, ~€100

Trenz electronic

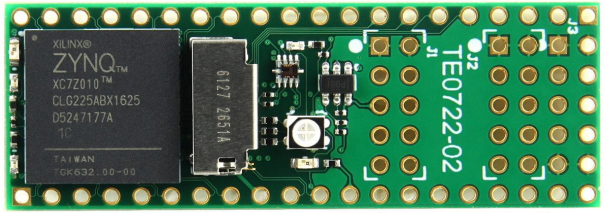


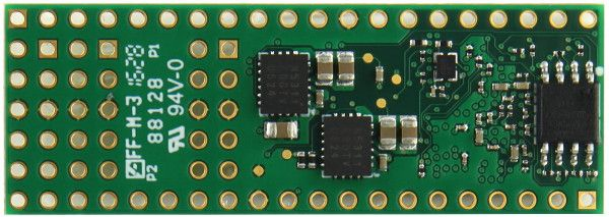
EBAZ4205, ~€10



2-Layer
640x480 VGA
115 MHz SDRAM

Muzy-2, BoM ~€10





shop.trenz-electronic.de

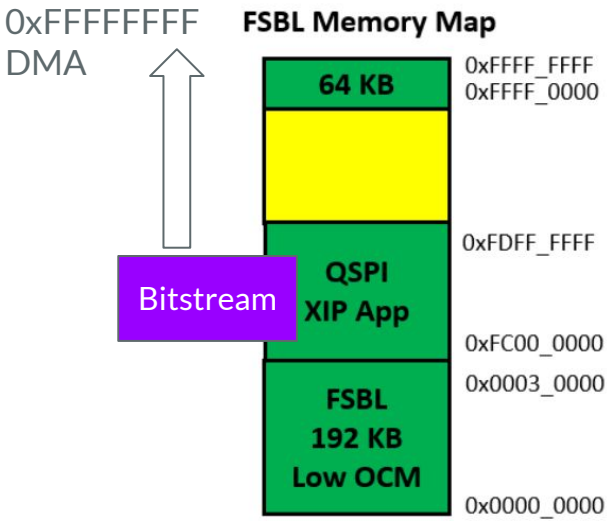
Photo Shows Similar Product

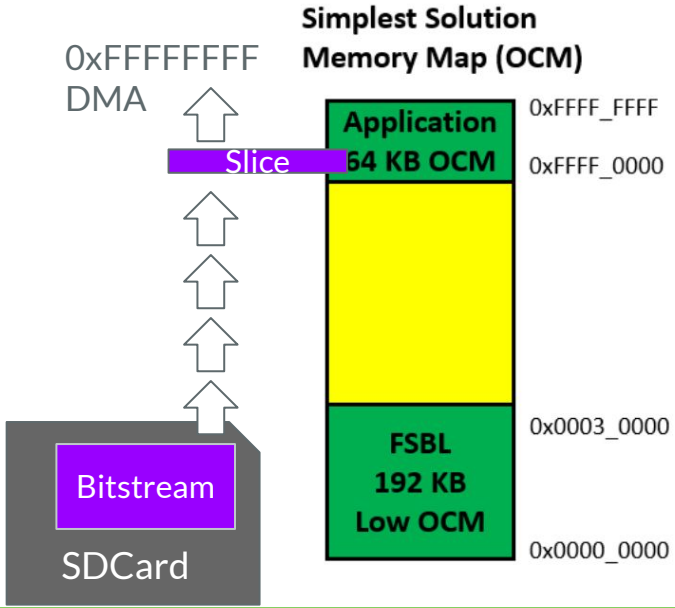
DIPFORTy1, ~€60

Trenz electronic

Possibilities unlocked

- **#1 No DDR SD Boot**
  - Not supported officially, *was* not convenient





https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/2418900993/Zynq+7000+Tips+and+Tricks

Possibilities unlocked

- **#2 Overclock 🔥**
- hz12opensource/libresdr
- GenZ

```
+cpu_mult_template='EMIT_MASKWRITE\(0XF8000100, 0x0007F000U ,0x000XX000U\),'
+cpu_mult_find='\s'"${cpu_mult_template/XX/(..)}"
+ddr_mult_template='EMIT_MASKWRITE\(0XF8000104, 0x0007F000U ,0x000XX000U\),'
+ddr_mult_find='\s'"${ddr_mult_template/XX/(..)}"
```

```
z7000_ps_param_900 = {
    'freq'  : { 'crystal'  : 33.333333333,
                'apu'      : 900.0
              }
    }
```

Flexibility meets more flexibility

- **#3 PL bitstream built on PS itself**
- It’s an ARM anyways
- OpenXC7 runs on 1 GB mem

https://www.youtube.com/watch?v=XkAzzpYiAUg

Larger devices

- **Zynq 7030, 7035, 7045, 7100 now supported by OpenXC7 + GenZ**
- Would have transceivers and PCIe blocks, DDR3 on PL, …

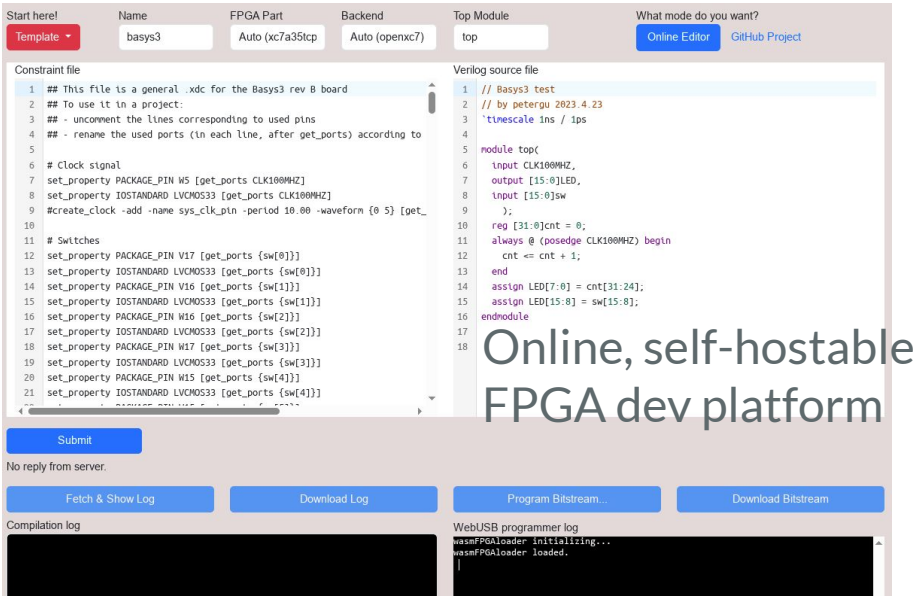
Future

Freedom is the future

- DDR3? PetaLinux? More IP cores?
- More IP cores w/ Open Source Toolchains?

PlutoSDR/Openwifi:
Why only on Xilinx FPGAs?

digikey.com



Online, self-hostable
FPGA dev platform

https://caas.symbioticeda.com/

Openwifi

release on CrowdSupply soon

Acknowledgement

OCP-TAP

LUG@USTC

VLAB@USTC

Thank you!

- github.com/regymm/GenZ
- github.com/openXC7