

Open Design Flows for Open Hardware Research

The ODE4EC Perspective

Christian Pilato

Politecnico di Milano

Luis Miguel Pinho

INESC TEC

Rene Scholz

IHP Microelectronics

Frank K. Gürkaynak

ETH Zurich

Luca Benini

ETH Zurich · Università di Bologna

Stefan Wallentowitz

Hochschule München



Open hardware is real — the path to silicon isn't open



Closed implementation

Tapeout still needs Cadence /
Synopsys

No open PDK at 28 nm



Fragmentation

Open tools exist, but don't
interoperate

AMS & verification: near-zero
open maturity



Usability & reproducibility

Workflows hard to reuse &
document

No open learning infrastructure

Open flows turn open tools into reusable workflows



Integration

Shared interfaces & standard formats

Front-end, back-end & verification interoperate



Verification

Simulation: Surfer · cocotb · Verilator

Formal: SymbiYosys · EQY equivalence



Automation

AI for RTL gen & design-space exploration

Modular flow integration · AI-assisted entry

Open tools + open flows = teachable, validated, transferable methodology

60+

Partner organisations

15

Countries

≈ €35M

Total funding · €19M EU + €16M national

ODE4EC-DIG

Digital SoC Design

- RTL → GDSII open flow
- Mainstream nodes · IP & memory
- Benchmarks & tapeouts

ODE4EC-PIV

Productivity · Interoperability · Verification

- Modular flow integration
- Simulation, formal & CI/CD
- AI-assisted design

ODE4EC-AMS

Analog & Mixed-Signal Design

- Mixed-signal methodologies
- AMS verification & validation
- Integration with digital flows

Integrated Open Design Infrastructure

Shared interfaces · Common APIs & automation · Reusable IP & benchmarks · Documentation & training · Governance & quality

Benefits: reusable IP · easier integration · faster exploration · reproducibility · accelerated research

From fragmented tools to one end-to-end flow



Today: fragmented

- HLS, P&R, GDSII tools don't interoperate
- No complete PDK support at 65-28 nm



DIG contributions

- Unified flow: Bambu · Dynamatic · YOSYS · OpenROAD
- Integration of PDK at 65-28 nm, tapeout-validated



Strategic objectives

- Full open RTL-to-GDSII flow
- Interoperability + memory / IP integration



Key KPIs

- $\leq 10\%$ PPA gap vs Cadence / Synopsys @ 28 nm
- 500+ users · 50+ external contributors

Coordinator: C. Pilato (POLIMI) — 23 partners — 10 universities · 5 RTOs · 7 SMEs · 1 LE

The connective tissue of open EDA



Modular frameworks

Typed DSLs: Spade · Chisel · MLIR
Integration: CIRCT · FuseSoC ·
CI/CD



AI-driven methods

LLM-assisted RTL & HW/SW
partitioning
AI-guided DSE for RISC-V SoCs



Verification & validation

cocotb · pyUVM · Verilator
simulation
Formal checks · CI/CD regression

Coordinator: L. M. Pinho (INESC TEC) — 22 partners — 10 universities · 4 RTOs · 9 SMEs · 1 LE

Open analog from near-zero to silicon

One open AMS flow: tools · PDK · IP verification · silicon validation



Analog & RF design flow

Analog/RF & AMS simulation

Parasitics & EM modeling



MOSAIC analog generation

Modular generator design

Reusable analog/RF IP



PDK setup & IP verification

Open PDK for mature nodes

Cross-domain validation



Commercial validation (MPW1)

Silicon validation via MPW

Full-platform evaluation

Coordinator: R. Scholz (IHP) — 26 partners — 9 universities · 6 RTOs · 6 SMEs · 5 LEs

Three streams, stronger together



Technical synergies

DIG-PIV: shared verification & CI/CD

Cross-stream roadmap via Coordination Board



Governance & community

Upstream-first: PRs to Yosys, OpenROAD, Bambu

FOSSi maintainer

Joint website and repository



EuroCDP integration

Tools pre-installed on cloud — no setup

EUROPRACTICE wafer access for EU

60+ European organisations · 2026–2029

The largest long-term multiplier



Education infrastructure

Open MOOCs on EUROPRACTICE —
no licence
Starter PDK + reference SoC ·
Docker/Nix
Summer schools & design challenge



Targets

≥ 300 students trained by M36
≥ 500 registered platform users
4+ open MOOCs published



Sustainability

Annual student tapeout via
EUROPRACTICE
Community governance post-project
CC-BY materials, reusable anywhere

Learner pipeline: Undergraduate → MSc / PhD → Industry & SME → Open community

An open invitation — join ODE4EC



Open research questions

- How close can open tools get to proprietary PPA?
- Where does ML-driven EDA help most?
- Can open EDA reach 7 nm / 5 nm long-term?



How to get involved

- Contribute code — PRs to Yosys, OpenROAD, Bambu
- Share CC-BY teaching materials & labs
- Use the ODE4EC flow in your course (Docker + TA kit)

ode4ec.eu · github.com/ode4ec · [ORConf 2026 Ghent](#) · [HiPEAC 2027](#)

Follow us!



Thank you

Open Design Flows for Open Hardware Research

ode4ec.eu



Funded by the
European Union

