## FPGA Continuous Integration and RISC-V Processor Design

Rodolfo Azevedo, Julio Nunes Avelar, Victor Prudente Lago and Angelo Renato Panzin Malaguti – UNICAMP - Brazil

**Challenge:** How do you select a new core for your Project?

Design a new core from Scratch

- Architecture/Specification
- Performance requirements

Buy one core

- Price/Licensing
- Performance

Use an open source model

• Which one should you use?

Git Clone

**IVerilog** 

We created a continuous integration for RISC-V processor to assess their maturity level using multiple FPGAs and synthesis tools.

Come to our poster to discuss and see several research opportunities

100+ cores available on riscv.org
How do I choose among them?

