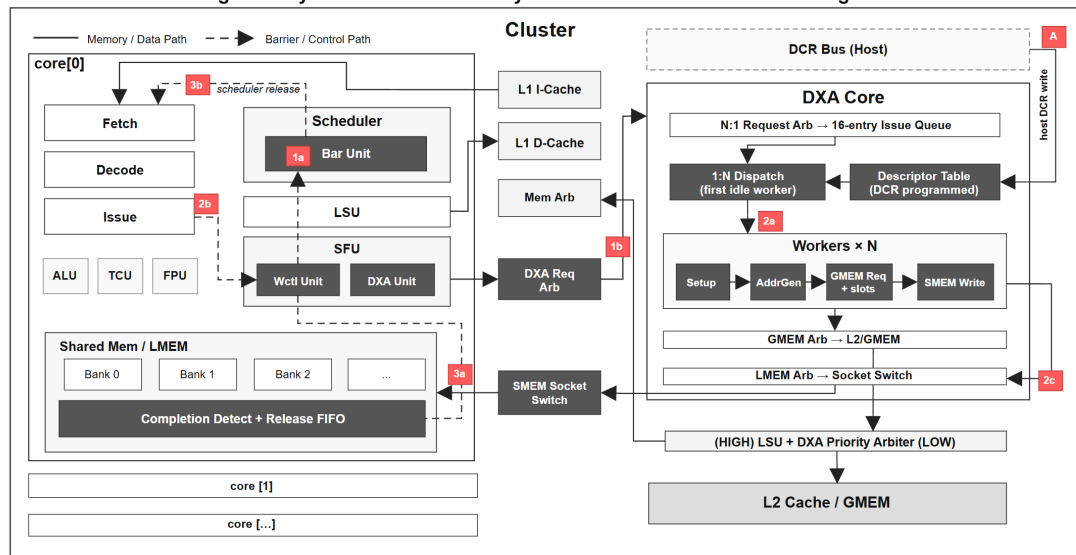


1. System Integration

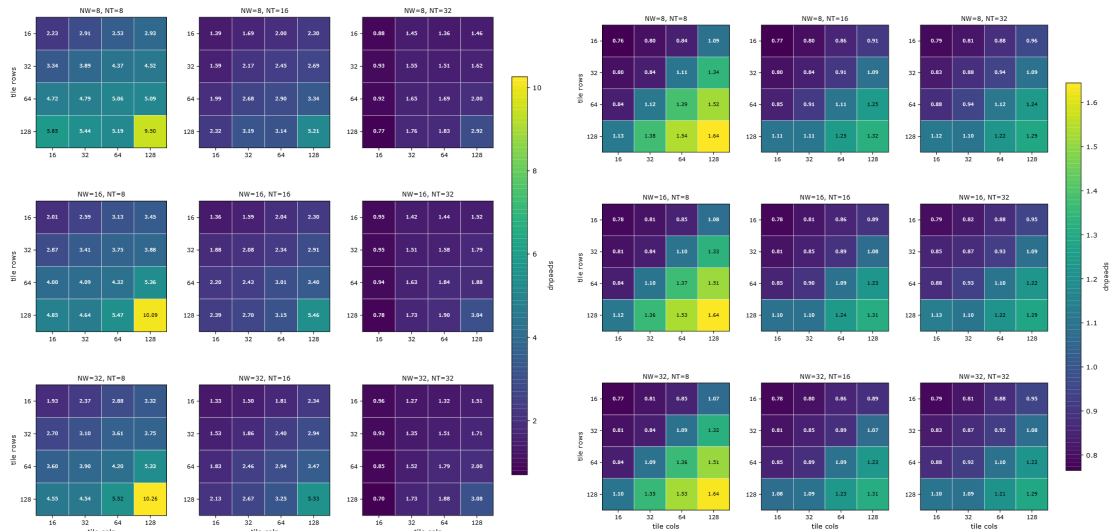
Figure 1. System-level DXA and asynchronous transaction-barrier integration



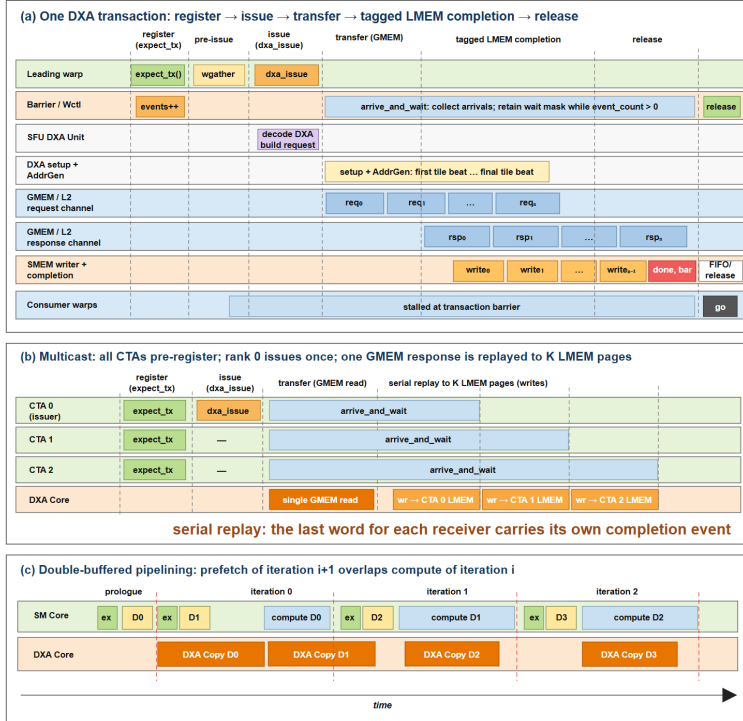
- DXA Core issues memory-centric work to many workers using barrier-controlled dispatch.
- Asynchronous barriers ensure correct consumption/production across GMEM and SMEM.
- Host programs DXA via DCR descriptors and observes completion via SMEM side logic

Figure 3(b): LSU / DXA speedup

Figure 3(c): per-CTA / multicast speedup



2. Execution Timelines



- Single transaction exposes the complete register → issue → transfer → release chain.
- Multicast replays one GMEM response to K LMEM receivers.

3. Evaluation

