

RPM: RISC-V Performance Model

Sahil Gandhi*, Hieu Mai, Anirudh Jain, Jiyong Yu, Vignyan Kothinti

An Open-source, Modular Framework for RISC-V Microarchitecture Modeling

Execution-Driven Simulation with True Wrong-Path Speculation

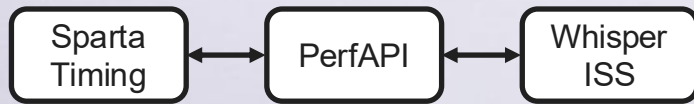
- Whisper ISS and the Sparta timing model advance together through **PerfAPI** – no full ISA in the timing model
- Executes every fetched instruction – true wrong-path speculation with real pollution and contention
- Hundreds of KIPS of simulation speed

Modular Interfaces for Design-Space Exploration

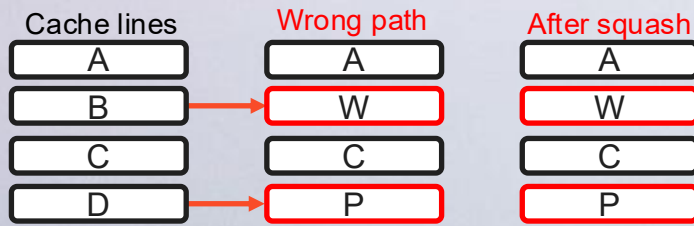
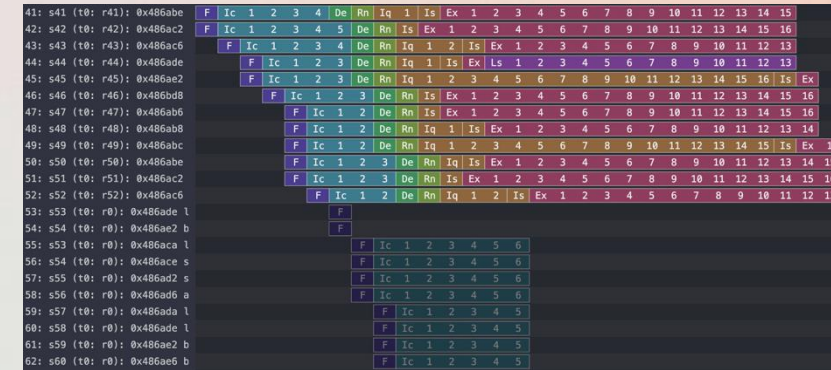
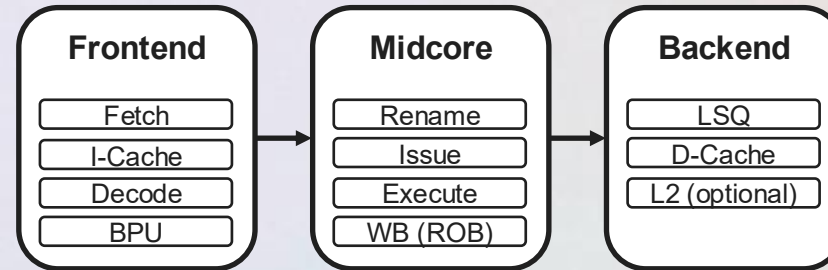
- Self-contained Sparta units linked by typed message ports
- Swap whole stages or drop in “perfect” models to isolate bottlenecks

An Ecosystem of Debugging Tools

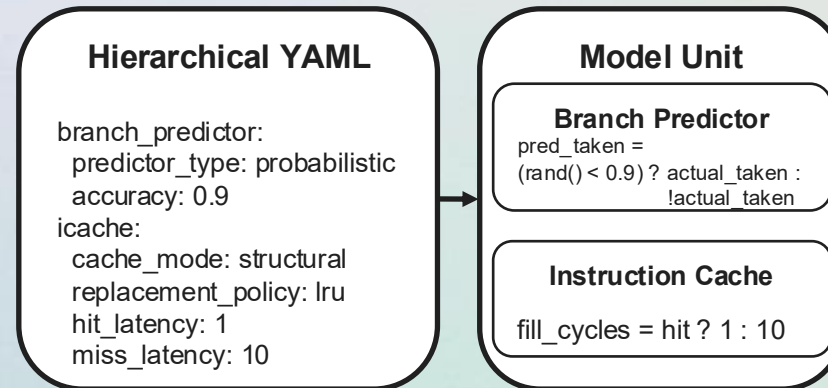
- AI-friendly structured logs
- Pipeline visualizer: per-cycle traces in popular formats (e.g., Kanata)
- Parallel sweeps on Slurm / AWS spot



Timing & functional state advance in lockstep



Cache pollution due to wrong-path speculation



Open-source on Github!

