# Open-Source FPGA Accelerator Artifacts for Sparse Workloads

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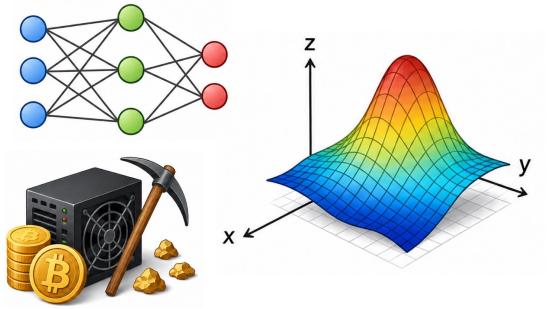
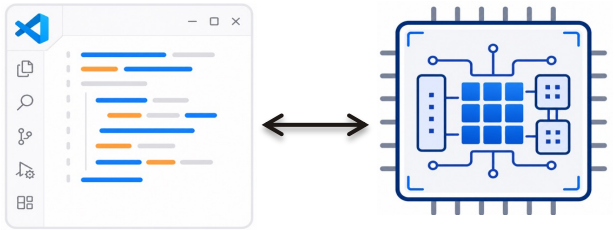
**Moore's Law drove decades of computing scalability**




**Modern sparse workloads expose the limits of traditional processors**



**FPGA combine SW stack with its reconfigurable fabric for acceleration**

**Our Contribution:** We release open-source artifacts of our three FPGA-based sparse accelerators: **Acamar**, **Chasoň** and **Procyon**. These artifacts expose the simulator, synthesizable hardware implementation, framework, and evaluation support, enabling the community to reproduce, inspect, and extend sparse accelerator designs.

## Acamar (MICRO 2024)

- ❑ Dynamically reconfigurable scientific computing accelerator
- ❑ **Artifact:** Cycle-level simulator used for Acamar evaluation
- ❑ **Impact:** Encourages novel techniques that leverage the partial dynamic reconfiguration capabilities of FPGAs

## Chasoň (MICRO 2025)

- ❑ Streaming accelerator for sparse algebra that support cross-HBM channel OoO data scheduling
- ❑ **Artifact:** Synthesizable HLS code for FPGA prototyping
- ❑ **Impact:** Advances remote memory-aware scheduling for multi-accelerator sparse systems

## Procyon (DAC 2026)

- ❑ Fine-grain multi-tenancy framework to support multiple sparse workloads within a single accelerator instance
- ❑ **Artifact:** Scheduling framework and HLS kernel for hardware integration
- ❑ **Impact:** Promotes research on SIMT-style multi-tenancy for sparse streaming accelerators to reduce total operational cost